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Process and Device Design, Experimental Characterization, and Modeling of RF LDMOSFETs on Silicon-on-Insulator Material

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13. ABSTRACT *(Maximum 200 words)*

A thorough analysis was performed to evaluate the advantage of power Ldmos RF transistors built on SOI substrate versus bulk silicon substrate. It had been anticipated a significant improvement would be realized with SOI due to the lower inherent parasitic capacitances. The disadvantage of SOI would be its inability to dissipate heat as well as bulk silicon.

Extensive data was taken to generate device models. RF simulations comparing simulated to actual verified these models.

Our observation is that at the frequency of 1 Ghz where the study was made, the advantage of lower parasitic capacitance is not apparent. There is an offset to this advantage due by the higher drain to gate feedback capacitance in the SOI process. The other disadvantage of SOI which is poorer heat dissipation played slightly to lower the performance.

Overall the results showed that at the frequency and power levels studied, SOI did not provide an advantage over bulk silicon devices.

Several publications have been derived from this work.

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1 INTRODUCTION

Silicon MOSFETs are increasingly finding applications at RF frequencies. This proliferation is a result of advances in processing technology and the introduction of new device structures that have allowed dramatic improvements in the voltage and power ratings of MOSFET devices, while significantly reducing parasitic elements [1-3]. Two basic MOSFET devices are used in RF sub-systems: the lateral double-diffused transistor (LDMOSFET) and the vertical double-diffused transistor (VDMOSFET). Typically VDMOSFETs are utilized in broadband, low-frequency applications, where they offer good stability. On the other hand, LDMOSFETs are used in narrowband, high-frequency applications, where higher gain is needed. Radio-frequency power MOSFETs are derivatives of conventional power devices used in high-speed power electronics [4,5]. The prime criterion for a power electronics device is its on-resistance; however, for RF applications power devices require minimal capacitance, which motivates modifications to the power MOSFET structure.

One type of enhancement that has attracted considerable interest for power electronics devices and signal-level RF transistors is silicon-on-insulator (SOI) substrates [6-9]. In this technology a buried dielectric (BOX) layer is inserted between the transistor and the bottom surface of the semiconductor die. Device fabrication thus occurs in a thin silicon film. The confinement by the BOX also eliminates much of the parasitic junction capacitance that is present in bulk devices. Lower capacitance enables faster switching, reduces switching losses, and can improve gain. An SOI device also exhibits better thermal ruggedness than a comparable bulk device since threshold voltage drift is greatly reduced. For these reasons SOI devices are being widely investigated for power electronics in high-temperature environments [10-12]; however, this interest has not yet extended to RF power applications.

We believe that RF power MOSFETs on SOI material can be developed into a significant improvement over state-of-the-art bulk silicon RF power devices. The inherent advantages of SOI (reduced capacitance and better thermal ruggedness) are highly desirable characteristics for RF power amplifiers. Moreover, the utility of SOI as a platform for monolithic integration of signal-level VLSI electronics and passive components suggests that SOI will be the leading technology for integrated power amplifiers [8,9,13].

This report summarizes the design, experimental characterization, and parameter extraction and matching of a 50-V radio-frequency (RF) lateral power MOSFET (LDMOSFET) in silicon-on-insulator (SOI) material. The device was fabricated using a 1.2-μm SOI CMOS process with minor modifications to accommodate specific features of the LDMOSFET, such as a body implant and an elongated drift region. Device design and wafer-level characterization were performed at the University of Illinois at Chicago (UIC). Packaging, amplifier design and test, and package-level characterization were performed by PolyFET RF Devices.

Twelve device variations were fabricated to bracket the expected performance of a principal device. The principal device was designed using finite-element numerical simulation methods (i.e. ATHENA and ATLAS). Beginning at the process level, the SOI CMOS recipe was adapted for the RF LDMOSFET. The device DC and RF characteristics were iteratively refined by tuning the process. The device three-dimensional structure was developed by considering the unique requirements of biasing the confined *p*-body region. Cell design was performed at UIC; computer entry of the layout was performed at PolyFET.

Following device fabrication, wafer-level characterization was performed at UIC and PolyFET. The measured DC and RF characteristics are presented later. Using the measured characteristics, model parameter extraction was performed. The model was entered into the HP EEsof Advanced Design System (ADS) microwave simulator for comparison with measured results. A reasonable match was obtained for both DC and RF characteristics. Comparison results are shown for simulations and modeling of the SOI devices as well as measured results of two similar commercial bulk devices (labeled L1C and L2B).

In each of the following sections that contain measured, simulated, or modeled data, a summary of results is included in the body of the text. More extensive data is attached as separate appendices for convenient reference. A concluding section is included which states the specific challenges presented during each phase of the design and characterization. It also offers some comments on design modifications that could be applied to boost the performance of this RF SOI LDMOSFET.

2 PROCESS AND DEVICE DESIGN

A total of twelve devices were fabricated, all variations on a single nominal device. Table 2.1 lists the key physical characteristics of devices. Q101 was the target structure. The discussion of process and device design pertains to Q101. All other devices, except Q103 and Q108, were obtained by scaling selected features (e.g. gate length or LDD length) in increments of 0.6 μm, which is the minimum mask step size. Q103 and Q108 had slightly more aggressive scaling values and deviated from the minimum mask step size.

TABLE 2.1 Device nomenclature and variability matrix.

Device Name	Drawn Gate Length (μm)	Drawn LDD Length (μm)
Q101	1.2	1.2
Q102	1.2	1.8
Q103	0.8	1.4
Q104	1.2	1.8
Q105	0.8	1.8
Q106[a]	1.2	1.8
Q107[b]	1.2	2.4
Q108	0.8	0.8
Q109[a]	1.2	1.8
Q110	1.2	1.8
Q111[c]	1.2	1.8
Q112[c]	1.2	1.8

a. All devices have a gate width of 1,252.8 μm, except Q106 and Q109 which are half-width.
b. Q107 has one fewer body tie.
c. Q111 and Q112 have enlarged contacts.

The processing sequence employed was derived from that of a standard 1.2-μm (drawn feature) SOI CMOS technology, with the addition of a p^- angle implant. This modification was made to create the LDMOSFET structure, which is illustrated in Fig. 2.1(b). Beginning with a p-type epitaxial substrate having a resistivity of 3,000 Ω-cm, a 500-Å gate oxide was grown. Then a boron implantation (3×10^{12} cm^2, 90 KeV) at a 45° slant was performed for V_T adjustment. The angle implantation energy and slant were optimized using finite-element numerical simulations (ATHENA) to produce a penetration under the gate of approximately 0.6 μm.

After the V_T adjust, the lightly-doped drain (LDD) feature was fabricated. This drift region is critical for achieving the desired breakdown voltage (50 V). The LDD was formed by an implant of arsenic (2×10^{12} cm^2, 80 KeV). The gate-to-drain overlap was also optimized through numerical simulation and harmonic balance simulation to achieve a compromise between fabrication yield (by increasing the

overlap) and the Miller feedback capacitance, C_{rss}, (by decreasing the overlap). An overlap of 0.1 μm was selected. Following the LDD, a TEOS spacer was fabricated.

Since the SOI structure confines the body region under the gate, a "striping" technique was employed to ground the body. This was accomplished by interleaving narrow p^+ body contact fingers into the usual n^+ source implant (see Fig. 2.1(a)). To ensure that the p^+ body contacts merge with the p body, as shown in Fig. 2.1(c), a slighter higher implant energy was used for p^+ formation to increase the depth. The cell layout density was improved by relying on the source self-aligned silicidation to electrically short the n^+ and p^+ regions, without requiring dedicated body contact openings. After several thermal steps for dopant activation and oxide densification, a conventional two-level metallization was performed.

The complete process recipe is stated in Table 2.2.

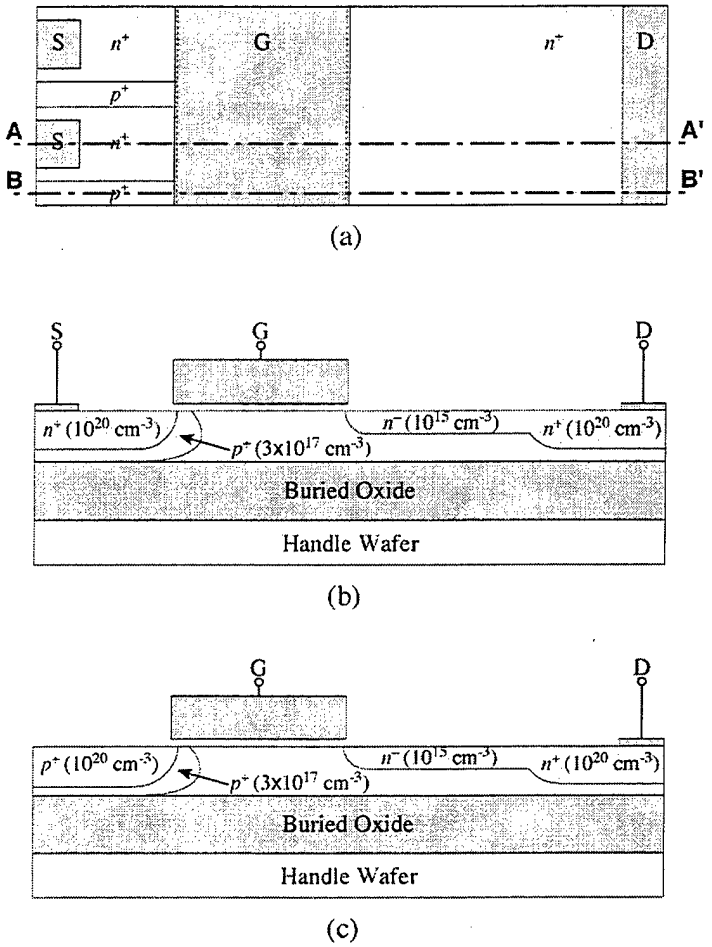


FIGURE 2.1 Schematic diagrams of the SOI LDMOSFET showing (a) its top view illustrating the striping of the body contact fingers, (b) a cross-sectional view at cutline *A-A'* through the MOSFET, and (c) a cross-sectional view at cutline *B-B'* through the *p*-body contact.

The results of the process simulation are shown in Fig. 2.2 in the form of a vertical cross-section (as taken through cutline *A-A'* of Fig. 2.1(a)). Corresponding vertical doping profiles are given in Fig. 2.3 for the intrinsic *p*-type epi under the gate, the center of the *p*-body region, the center of the LDD region, and under the drain electrode.

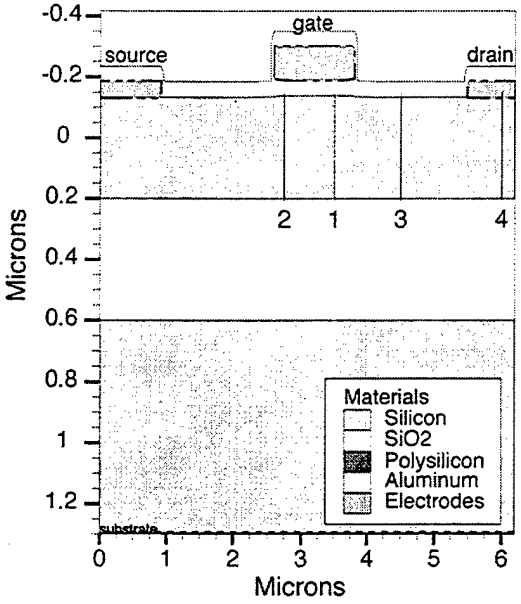


FIGURE 2.2 Actual device vertical cross-section obtained from process simulation Four cutlines are labeled. These are the locations of the doping profiles shown in Fig. 2.3.

This structure was imported directly into the 2-D numerical device simulator. The only modification to the structure was the addition of a *p*-body electrode to model the effect of the p^+ body tie. Since the primary MOSFET cross-section (cutline *A-A'*) does not include the body ties, this modification was necessary to set the bias on the *p*-body. The electrode was placed on the top surface of the buried oxide and its extent was entirely contained within the *p*-body region. The adjacent n^+ source and *p*-epi were allowed to assume arbitrary potentials at the buried oxide-silicon interface.

The results of the device simulation are contained in Appendix A. Its contents consist of the following waveforms. Bias conditions are noted as appropriate. All 2-D simulations were performed for 280K, 300K, 350K, and 400K.

Name	Conditions
Drain-source static breakdown (BV_{ds})	V_{gs} = 0 V; V_{ds} = swept
Threshold voltage (V_T)	V_{ds} = 0.1,10 V; V_{gs} = 0–6 V
Transconductance versus gate bias (g_m-V_{gs})	V_{ds} = 7.5 V; V_{gs} = 0–6 V
Maximum transconductance versus drain bias ($g_{m,max}$-V_{ds})	V_{ds} = 2–14 V; V_{gs} = 0–6 V
Forward conduction (I_d-V_{ds})	V_{ds} = 0–18 V; V_{gs} = 2,3,4,5,6 V
Scattering parameters (S_{11} and S_{22})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 10 MHz – 2.9 GHz
Scattering parameters (S_{12} and S_{21})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA f = 10 MHz – 2.9 GHz

The $g_{m,max}$-V_{ds} plot was obtained by noting, for each drain bias, the maximum transconductance that obtains by varying the gate voltage 0–6 V. It is intended to show the gain flatness as an aid in determining a suitable RF bias point.

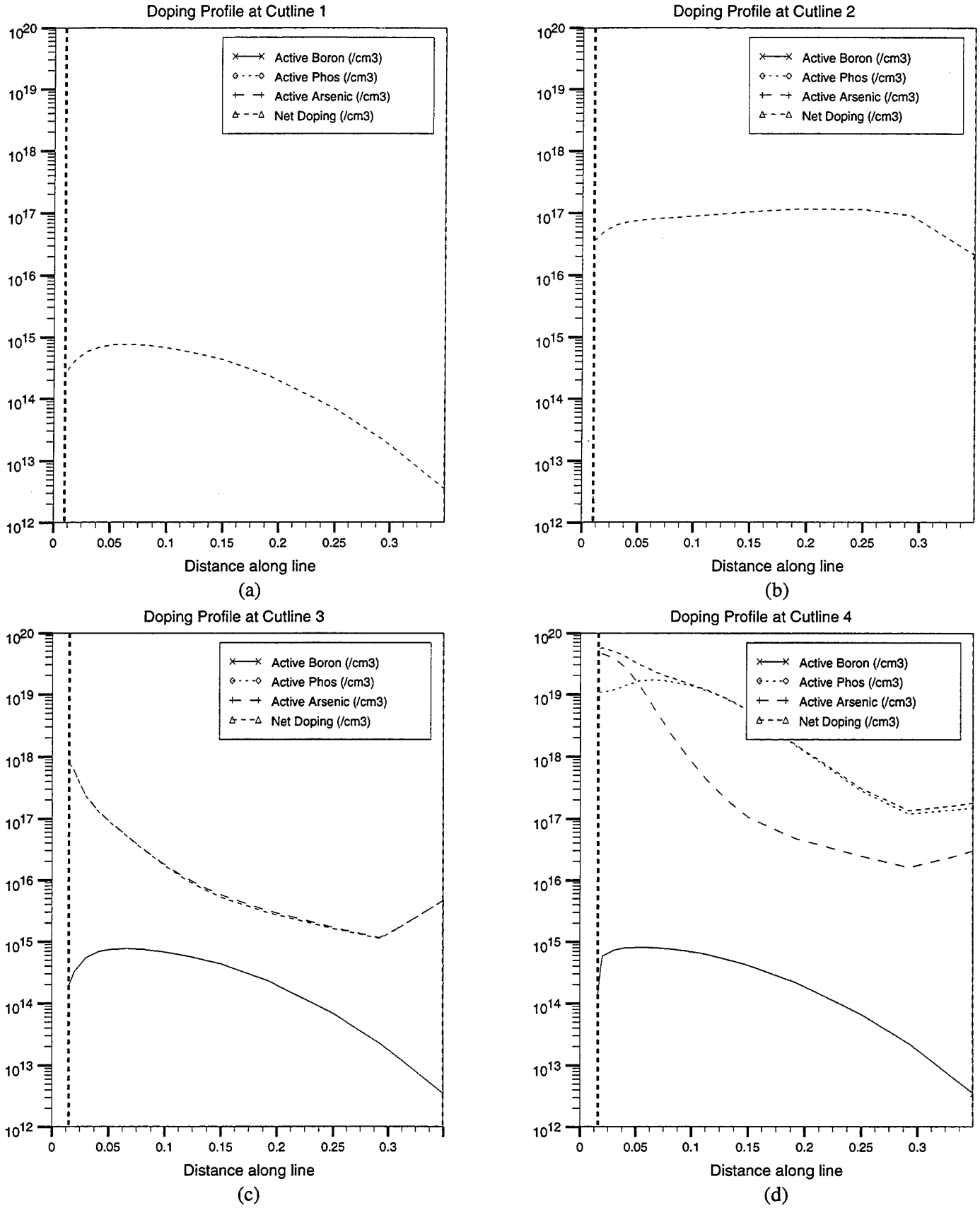


FIGURE 2.3 Device vertical doping profiles taken at cutlines through the (a) p-epi, (b) p-body, (c) LDD, and (d) n^+ drain regions. The locations of the cutlines are identified in Fig. 2.2.

TABLE 2.2 Process recipe for the 50-V RF SOI LDMOSFETs.

Step	Name	Thickness	Dopant, Dose, Energy	Temperature, Time
1	Oxide growth	400 Å		850 °C, 20 min.
2	Island mask			
3	Island etch			
4	Unused			
5	Unused			
6	Oxide deposition and anneal			900 °C, 20 min.
7	Active area mask			
8	Active area etch (wet)			
9	Gate oxide deposition	500 Å		
10	Polysilicon deposition			
11	Polysilicon doping		Phosphorous, 3×10^{15} cm^2 80 KeV	
12	Polysilicon mask			
13	Polysilicon etch			
14	p^- body mask			
15	p^- body angle implant		Boron, 3×10^{12} cm^2 90 KeV (45° tilt)	
16	Unused			
17	LDD blanket implant		Arsenic, 2×10^{12} cm^2 80 KeV	
18	Re-oxidation			900 °C, 30 min.
19	p^+ mask			
20	p^+ implant (body ties)		BF_2, 5×10^{15} cm^2	
21	TEOS			
22	Etch spacer			
23	n^+ mask			
24	n^+ implant		Phosphorous, 2×10^{14} cm^2 85 KeV	
25	n^+ implant		Arsenic, 2.1×10^{14} cm^2 85 KeV	
26	Oxide deposition	1,000 Å		
27	RTA			1050 °C, 0.5 min.
28	Oxide densify (in steam)			850 °C, 6 min.
29	Silicide block mask			
30	Silicide block etch			
31	Cobalt deposition			
32	First silicide anneal			RTA
33	Selective etch			
34	Second silicide anneal			RTA
35	Oxide/BPSG deposition			
36	Oxide densify			900 °C, 20 min.
37	Contact mask			
38	Contact etch			
39	Metal 1 deposition			
40	Metal 1 mask			

41	Metal 1 etch			
42	ILD 1 TEOS			
43	SOG			
44	SOG cure			
45	Etch back			
46	ILD 2 TEOS			
47	Via mask			
48	Via etch			
49	Metal 2 deposition			
50	Metal 2 mask			
51	Metal 2 etch			
52	Passivation			
53	Pad mask			
54	Pad etch			
55	Alloy			
56	Back side grind			
57	Back side gold			

3 MASK DESIGN

3.1 Introduction and Purpose

The design rules followed were those of an SOI CMOS technology, as provided by Allied Signal. The RF SOI LDMOSFET design conformed to the relevant NMOS design rules. Some of the design rules were violated as they were not applicable to discrete devices. We adjusted the gate length minimum feature size from 1.2 μm to 0.8 μm for evaluation purposes.

The basic structure of the RF SOI LDMOSFET matches that of the one used for the bulk silicon test structure. The bond pads were arranged for on-wafer probing capability. The device size is 1,252 μm in width for the SOI versus 1,440-μm width for the bulk silicon device.

An array of test structures, Q101-Q112, was created to test various structure dimensional effects on RF performance. Table 3.1 defines the designs and splits of these structures. A set of standard test structures was also included for process monitoring. These are identified in Table 3.2.

TABLE 3.1 Definition of the device structure variations for Q101 to Q112.

Device	Gate length (μm)	LDD length (μm)	Metal Route	Remarks
Q101	1.2	1.2	Source metal over top	Contact inside block by 1.2 μm. Block inside n^+ by 1.6 μm.
Q102	1.2	1.8	" "	Gate width = 52.2*2*12 μm = 1252.8 μm = 0.12528 cm. Contact inside block by 0.8 μm. Block inside n^+ by 0.8 μm.
Q103	0.8	1.4	" "	Contact inside block by 1.2 μm. Block inside n^+ by 1.6 μm.
Q104	1.2	1.8	" "	Contact to gate space 1.6 μm (rule = 2.0 μm). Contact inside block by 1.2 μm.
Q105	0.8	1.8	" "	Contact inside block by 1.2 μm. Block inside n^+ by 1.2 μm.
Q106	1.2	1.8		1/2 gate width of Q104.
Q107	1.2	2.4		One fewer body tie than Q102.
Q108	0.8	0.8	" "	Contact inside block by 1.2 μm. Block inside n^+ by 2.2 μm.
Q109	1.2	1.8		Q104 but half gate width (W = 0.0626 cm).
Q110	1.2	1.8		Q104 but drain n^+ away from island edge.
Q111	1.2	1.8		Q104 but with long contacts. Violates via to contact space rule.
Q112	1.2	1.8		Q104 but with long contacts and long via. Violates via to contact space rule.
Q101-array	1.2	1.2		Gate width = 104.4*2*18 μm = 1879.2*2 μm = 0. 37584 cm. Using 2 cells final transistor = 0.75168 cm
Q102-array	1.2	2.4		Gate width = 104.4*2*18 μm = 1879.2*2 μm = 0. 37584 cm. Using 2 cells final transistor = 0.75168 cm
Q103-array	0.8	1.4		Using Q103 for array.
Q104-array	1.2	1.8		Using Q104 for array.
Q105-array	0.8	1.8		Using Q105 for array.

TABLE 3.2 Definition of the process test structure variations.

Diodes
p^+/n^+
p-well/n^+
LDD/p^+
LDD/p-well
4-Point Probe Resistors
Silicided polysilicon.
Silicided p^+ polysilicon
Silicided n^+ polysilicon
Silicided p^+ in epitaxial layer
Silicided n^+ in epitaxial layer
n^+ doped polysilicon
Undoped polysilicon
p^+ resistance
n^+ resistance
p-well resistance
LDD resistance
Large Areas for SRP
n^+
p^+
p-well
LDD
Capacitors
Large capacitor - gate oxide
Poly to metal 1
Metal 1 to metal 2
R-C Chains
n^+ doping
p^+ doping

4 WAFER-LEVEL TESTING

4.1 Introduction

Wafer-level characterization was performed at UIC and PolyFET. The instrumentation at UIC includes a Cascade Microtech Summit 12000 wafer probe station, a Hewlett-Packard (HP) 4156B precision semiconductor parameter analyzer, and an HP 8753ES 6-GHz vector network analyzer (VNA). All characterization performed at UIC was conducted at room temperature (300K).

The data presented below consists of two types: DC static characteristics and RF two-port scattering (S) parameters. Measurements were performed at three die sites across the wafer. The wafer map and the selected die sites are shown in Fig. 4.1. The three die sites were chosen to observe the process variability across the wafer. Significant variations in device performance were observed, as discussed later.

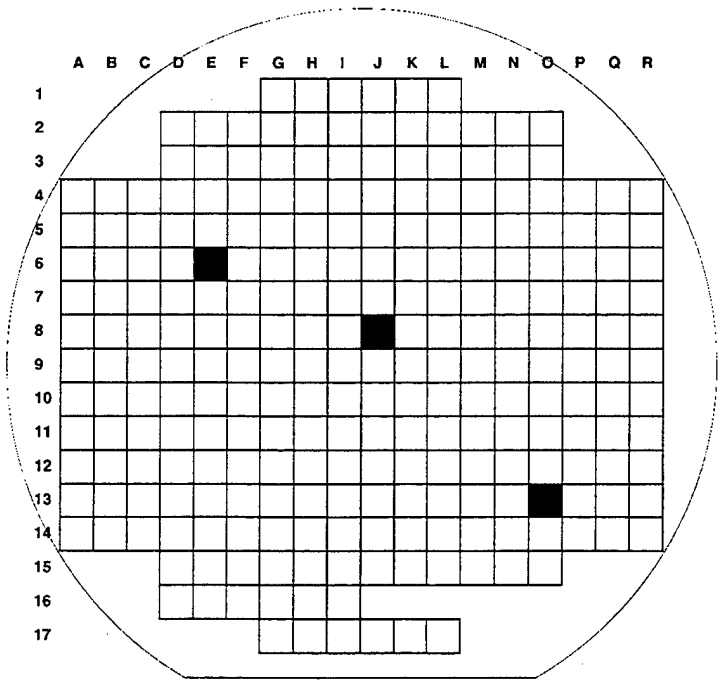


FIGURE 4.1 Wafer map and nomenclature. Die sites selected for measurement are indicated in black. The wafer flat is at the lower edge of the picture.

The results of the device measurements are contained in Appendix B. Its contents and the pertinent bias conditions are discussed in more detail in the following subsections.

4.2 DC Static Characteristics

The DC characterization was performed using full Kelvin contacts to probe pads on the wafer surface. The Kelvin contacts ensured that cable parasitics were extracted from measured characteristics and that meter biasing was calibrated to on-wafer conditions. Table 4.1 lists the DC measurements performed and their conditions.

TABLE 4.1 Definition and conditions of the DC measurements.

Name	**Conditions**
Drain-source static breakdown (BV_{ds})	V_{gs} = 0 V; V_{ds} = swept
Threshold voltage (V_T)	V_{ds} = 0.1,10 V; V_{gs} = 0–6 V
Transconductance versus gate bias (g_m-V_{gs})	V_{ds} = 7.5 V; V_{gs} = 0–6 V
Maximum transconductance versus drain bias ($g_{m,max}$-V_{ds})	V_{ds} = 2–14 V; V_{gs} = 0–6 V
Forward conduction (I_d-V_{ds})	V_{ds} = 0–15 V; V_{gs} = 2,3,4,5,6 V
Scattering parameters (S_{11} and S_{22})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 10 MHz – 3 GHz
Scattering parameters (S_{12} and S_{21})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 10 MHz – 3 GHz
Unity current gain frequency versus drain current (f_T-I_d)	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA

The $g_{m,max}$-V_{ds} plot was obtained by noting, for each drain bias, the maximum transconductance that obtains by varying the gate voltage 0–6 V. It is intended to show the gain flatness as an aid in determining a suitable RF bias point.

Sample measured (wafer-level) waveforms obtained for devices Q101 and Q103 are presented in Figs. 4.2 and 4.3 below. Q101 was selected since it was the nominal device. Q103 was selected since it exhibits, as will be shown later, the best RF performance. Table 4.2 summarizes the key measured DC characteristics.

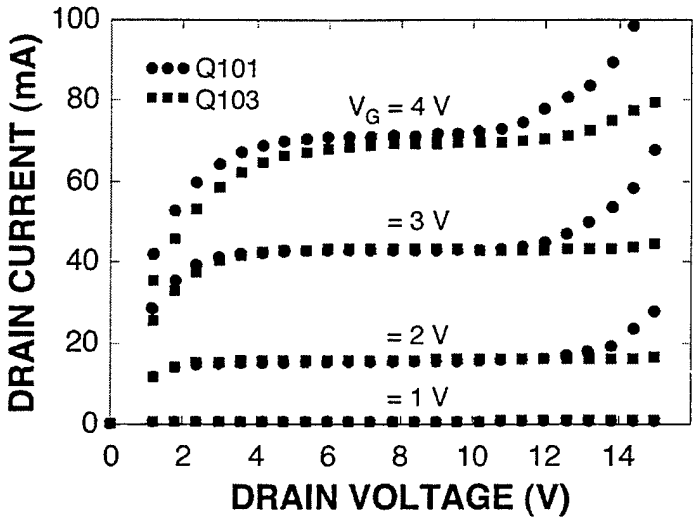


FIGURE 4.2 Measured I_d-V_{ds} characteristics.

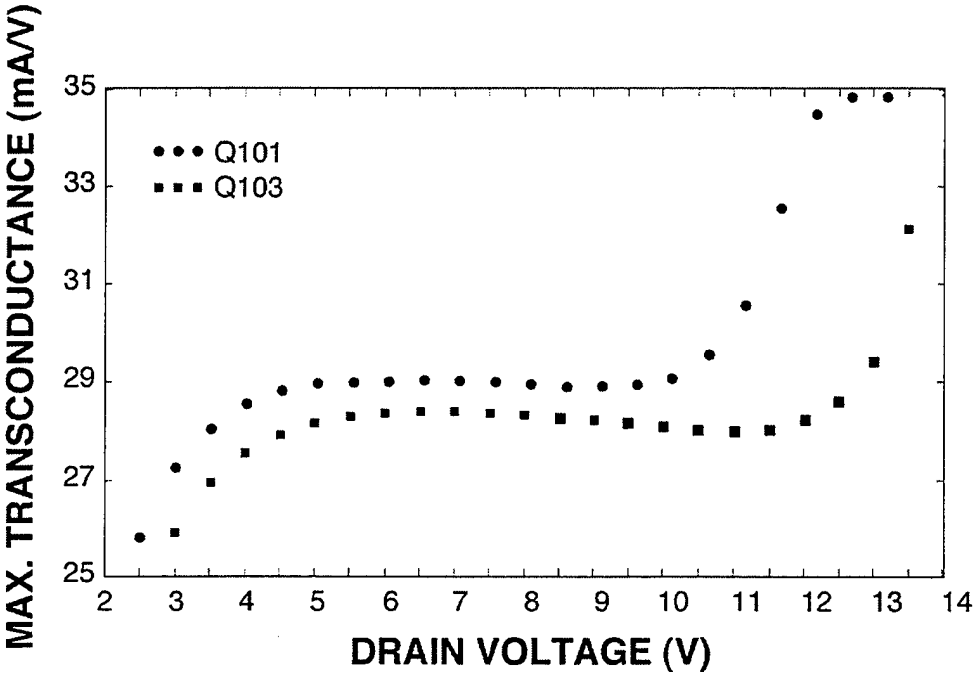


FIGURE 4.3 Measured g_m-V_{ds} characteristics.

TABLE 4.2 Summary of key measured DC characteristics.

Symbol	Definition/Purpose	Measurement Conditions
BV_{dss}	Drain-source breakdown voltage	V_{gs} = 0 V
I_d-V_{gs}	Subthreshold leakage to moderate inversion	V_{ds} = 0.1 V and V_{ds} = 10 V
I_d-V_{ds}	Conduction curves	V_{ds} swept 0 V to 15 V, V_{gs} swept 1 V to 4 V
g_m-V_{gs}	Small-signal gain as a function of gate bias	V_{ds} swept 3 V to 12.5 V
g_m-V_{ds}	Maximum small-signal gain as a function of drain bias	

4.3 Scattering Parameter Characteristics

The RF characterization was performed using coplanar waveguide probes within an EMI- and light-free hood. Calibration to the probe pads was obtained using an impedance standard substrate (ISS) and the short-open-load-thru (SOLT) methodology. Table 4.3 lists the RF measurements performed and their conditions. Sample waveforms are shown in Figs. 4.4 and 4.5.

TABLE 4.3 Definition and conditions of the RF S-parameter measurements.

Symbol	Definition/Purpose	Measurement Conditions
S_{11}, S_{22}	Input and output reflection coefficients	V_{ds} = 7.5 V and I_d swept 5 mA to 100 mA and V_{gs} = 3 V and V_{ds} swept 2.5 V to 3.5 V
S_{21}, S_{12}	Forward and reverse transmission coefficients	V_{ds} = 7.5 V and I_d swept 5 mA to 100 mA and V_{gs} = 3 V and V_{ds} swept 2.5 V to 3.5 V
$\|h_{21}\|$–f	Current gain as a function of frequency	V_{ds} = 7.5 V and I_d swept 5 mA to 100 mA and V_{gs} = 3 V and V_{ds} swept 2.5 V to 3.5 V
f_T-I_d	Unity current gain as a function of drain bias	

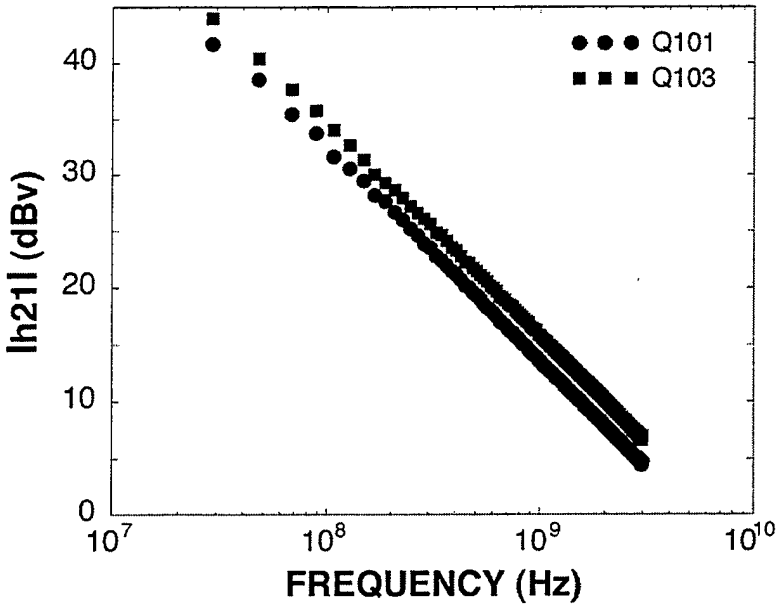


FIGURE 4.4 Measured current-gain–frequency characteristics (at V_{ds} = 7.5 V and I_d = 25 mA).

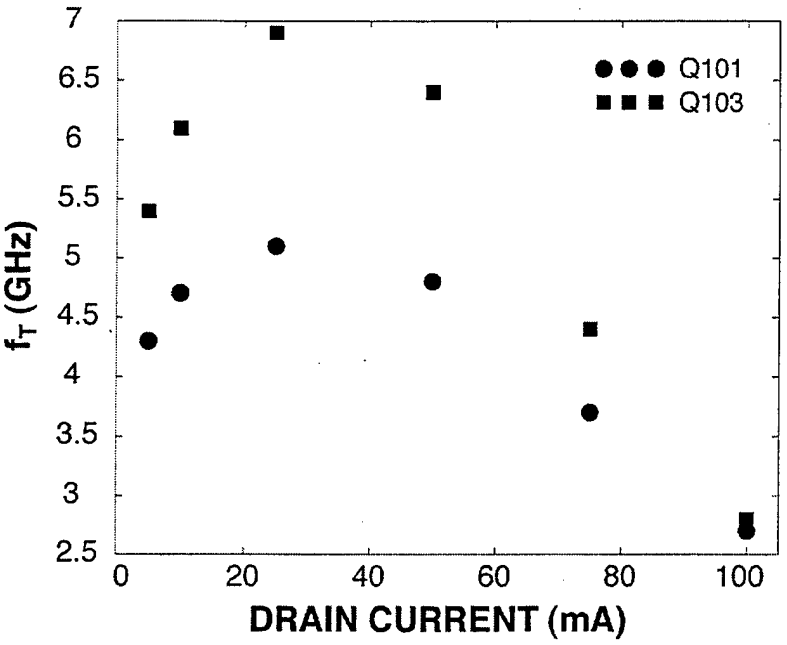


FIGURE 4.5 Measured f_T-I_d characteristics.

5 PACKAGE-LEVEL TESTING

5.1 Introduction and Purpose

The test structures were packaged in the Polyfet "AP" package. This package is used for the PolyFET product LP801 on which we have done extensive analysis in the past. The AP package is a quarter-inch square ceramic-based carrier mounted on a copper-tungsten flange. A detailed mechanical layout of this package can be found in the data sheet for LP801 part.

Unlike the standard bulk LDMOS devices, the bottom surface of the SOI die is floating. The bulk devices have the bottom surface of the die shorted to the source electrode, and the source is therefore attached directly to the heat sink. For the SOI device, bond wires are required to connect the source bond pad to the carrier in order to access the source of the chip. The added bond wires have a negative impact on the RF performance of the chip and this can be seen in the drastic difference in the S-parameters between wafer level measurement and package level measurement, as shown in Fig. 5.1.

5.2 Results and Discussion

The effects of the added inductance are most significant in the curves of S_{11} and S_{22}. A comparison of the wafer level versus packaged unit in RF performance can be seen in the following G_{max} plot (refer to Fig. 5.2).

5.3 Amplifier Design

In order to design an amplifier to measure the P_{in}-P_{out} performance of the packaged unit, a Spice model for the transistor was developed. The Spice model was derived from S-parameter measurements, DC IV curves, and capacitance data. The Spice model arrived at is listed in Table 5.1. A photograph of the constructed amplifier is shown in Fig. 5.3.

Following, in Fig. 5.4, is the measured P_{in}-P_{out} data of the built amplifier. Input and output matching were performed to obtain highest efficiency. Matching was simulated using HP-EEsof Libra software. The measured data are very close to simulated results. The performance is similar to that of a comparative bulk device, which is shown in Fig. 5.5.

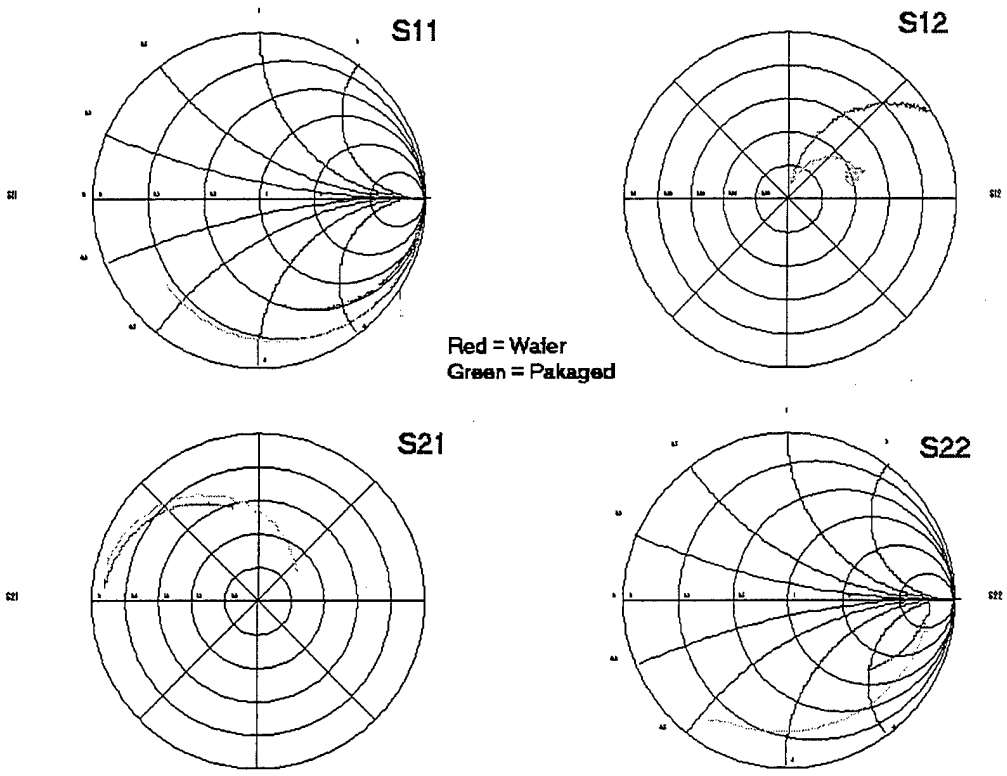


FIGURE 5.1 Comparison of wafer- and package-level S-parameters.

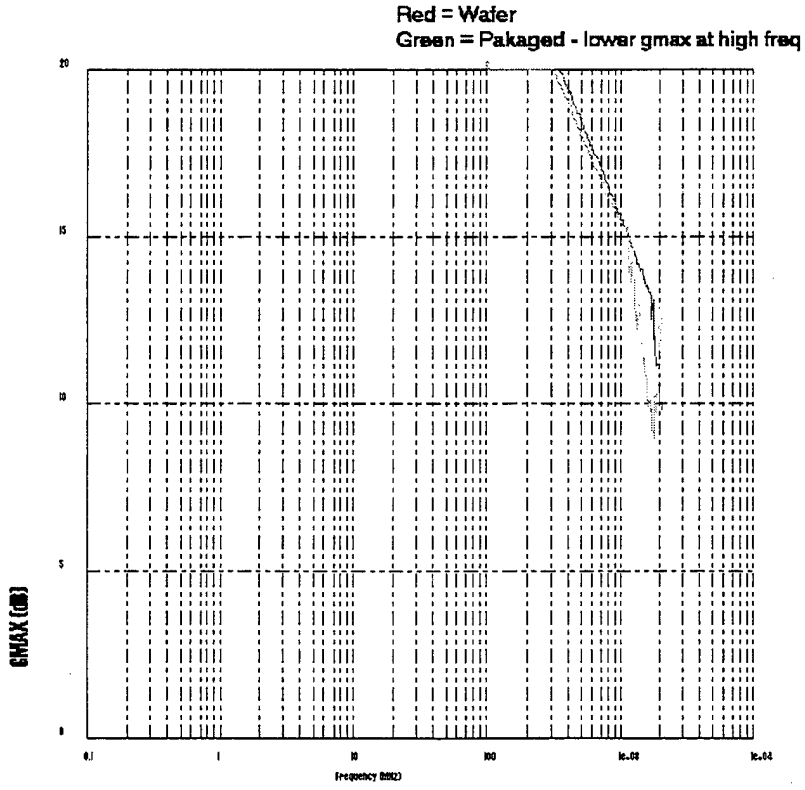


FIGURE 5.2 Comparison of wafer- and package-level G_{max}.

TABLE 5.1 Spice model developed for the packaged amplifier.

```
*POLYFET RF DEVICES,   02/14/00
*PHONE:(805)484-4210; FAX:(805)3393  CONTACT: MR. S.K. LEONG
*HIGH POWER, HIGH FREQUENCY, RF N-CHANNEL DMOS MOSFET
*NOTE:-HP/EESOF USES 'GATE DRAIN SOURCE' ORDER
*                D G S
.SUBCKT  Q101    /PF 20 10 30
LGATE 10  11    0.292N
RGATE 11  12    6.92
CG    10  30    0.017P
CRSS  12  17    0.0125P
CISS  12  14    2.25P
LS    14  30    0.293N
CS    14  30    0.723P
LD    17  20    0.018N
CD    20  30    0.006P
R_RC  16  17    261
C_RC  14  16    3.74P
MOS   13  12  14  14    Q101MOS  L=1.2E-6 W=1252E-6 ;D G S B LEVEL1
JFET  17  14  13        Q101JF                ;D G S
DBODY 14  17            Q101DB                      ;P N
.MODEL   Q101MOS NMOS(VTO=1.4 KP=0.9E-5 LAMBDA=0.15 RD=8.0 RS=9.0)
.MODEL   Q101JF  NJF (VTO=-5.25 BETA=6.0 LAMBDA=1)
.MODEL   Q101DB  D   (CJO=4.0P  RS=0.25 VJ=12.0 M=0.2 BV= 16.0)
.ENDS
```

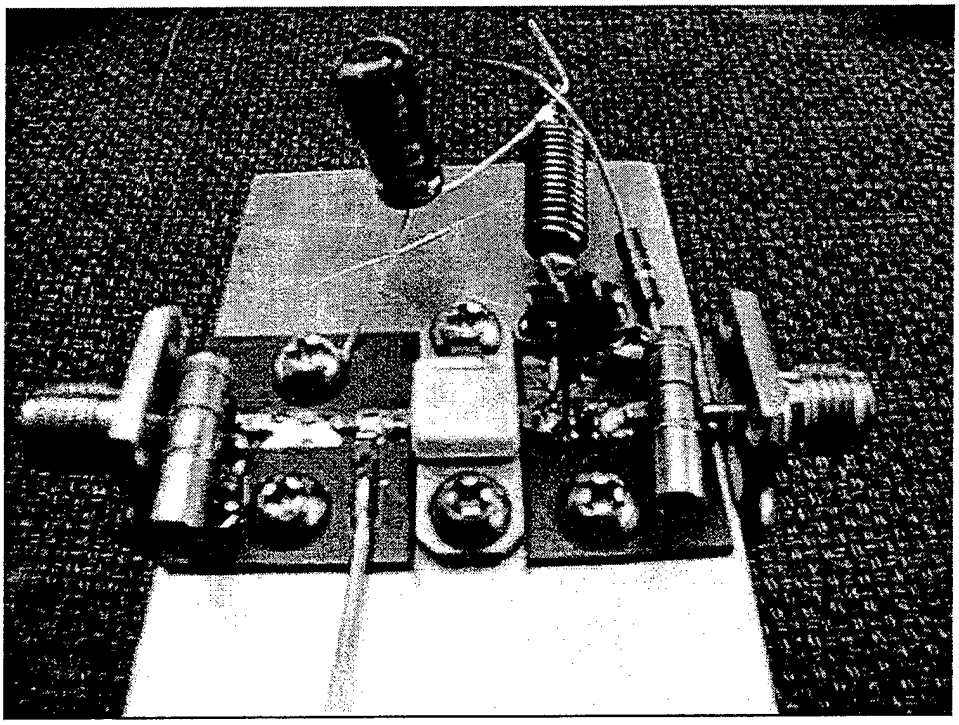


FIGURE 5.3 Photograph of the constructed RF amplifier.

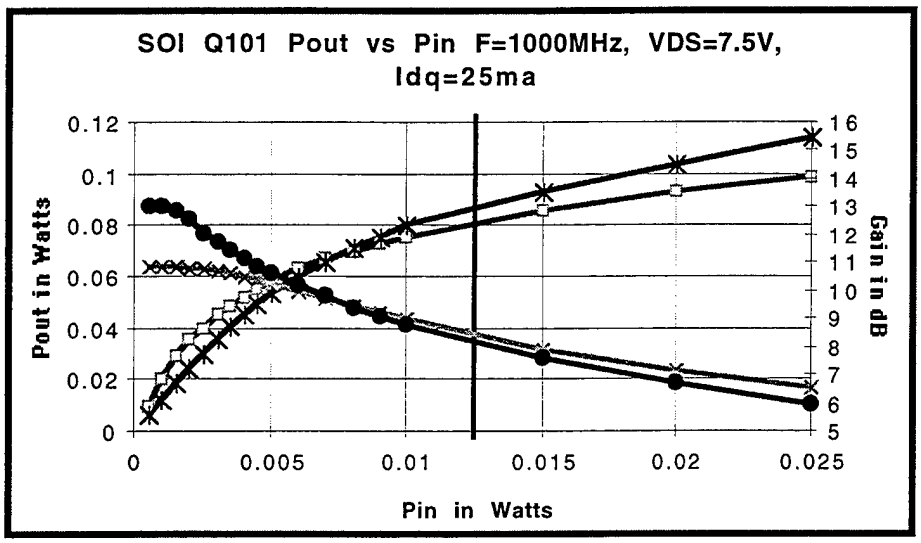


FIGURE 5.4 P_{in}-P_{out} measured data of the SOI LDMOSFET RF amplifier.

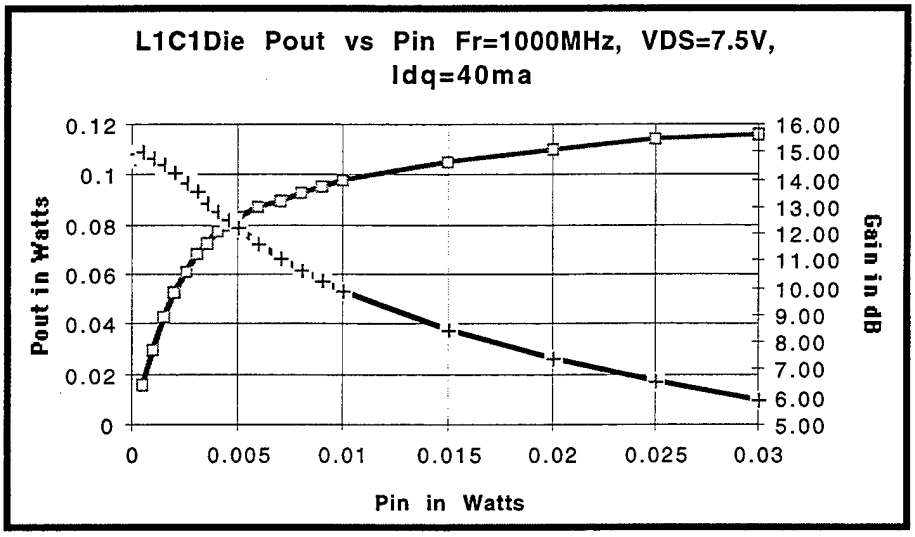


FIGURE 5.5 P_{in}-P_{out} measured data of a comparative bulk LDMOSFET RF amplifier.

6 COMPARISON OF MEASURED AND SIMULATED RESULTS

6.1 Introduction and Purpose

Following DC and RF characterization of the fabricated parts, detailed re-simulations were performed to match the measured performance and identify specific process variations that may be responsible for differences in the designed-for and measured results. Appendix D lists comprehensive overlay plots of several comparison devices. The list of devices is stated in Table 6.1. The overlay plots, and their bias conditions, are listed in Table 6.2.

TABLE 6.1 Definition of waveforms in overlay plots.

Label	Definition/Purpose
Q101: 2D simulation	Original designed device using 2D numerical simulation
Q101: measured	Measured (wafer-level) results of device Q101
Q103: measured	Measured (wafer-level) results of device Q103
Q101: 2D matched	Revised 2D simulations matched to measured Q101 results
Q103: 2D matched	Revised 2D simulations matched to measured Q103 results
Q101: ADS matched	Revised ADS modeling matched to measured Q101 results
Q103: ADS matched	Revised ADS modeling matched to measured Q103 results
Q101 (packaged): measured	Measured (package-level) results of device Q101
Q103 (packaged): measured	Measured (package-level) results of device Q103
L1C (packaged): measured	Measured (package-level) results of bulk device L1C
L2B (packaged): measured	Measured (package-level) results of bulk device L2B

TABLE 6.2 Definition and conditions of the overlay plots.

Name	Conditions
Drain-source static breakdown (BV_{ds})	V_{gs} = 0 V; V_{ds} = swept
Threshold voltage (V_T)	V_{ds} = 0.1,10 V; V_{gs} = 0–6 V
Transconductance versus gate bias (g_m-V_{gs})	V_{ds} = 7.5 V; V_{gs} = 0–6 V
Forward conduction (I_d-V_{ds})	V_{ds} = 0–18 V; V_{gs} = 2,3,4,5,6 V
Scattering parameters (S_{11} and S_{22})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 100 MHz – 2.1 GHz
Scattering parameters (S_{12} and S_{21})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 100 MHz – 2.1 GHz

7 MODEL PARAMETER EXTRACTION AND MATCHING

7.1 Introduction and Purpose

The wafer-level device was modeled in the HP EEsof ADS using the equivalent circuit shown in Fig. 7.1. The extracted model parameters are listed in Table 7.1. Sample comparison data is shown in Figs. 7.2 and 7.3 for DC conditions and in Fig. 7.4 for RF conditions.

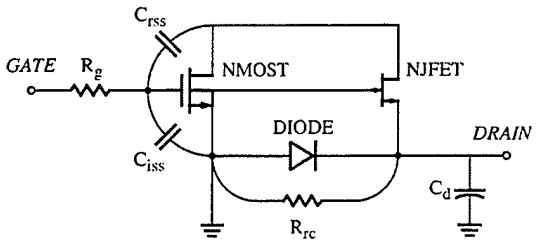


FIGURE 7.1 Circuit simulation model.

TABLE 7.1 Extracted model parameters.

Parameter	Extracted Value
MOSFET	
V_{t0} (V)	0.6
k_p (μS)	25
μ_0 (cm^2/V-sec)	300
v_{sat} (m/s)	6.8×10^4
JFET	
V_{toj} (V)	–7.4
ß (S)	6
DIODE	
C_{j0} (pF)	0.8
R_s (Ω)	250
PARASITICS	
C_{rss} (pF)	0.1
C_{iss} (pF)	1.0
C_d (pF)	0.4
R_g (Ω)	7
R_{rc} (kΩ)	10

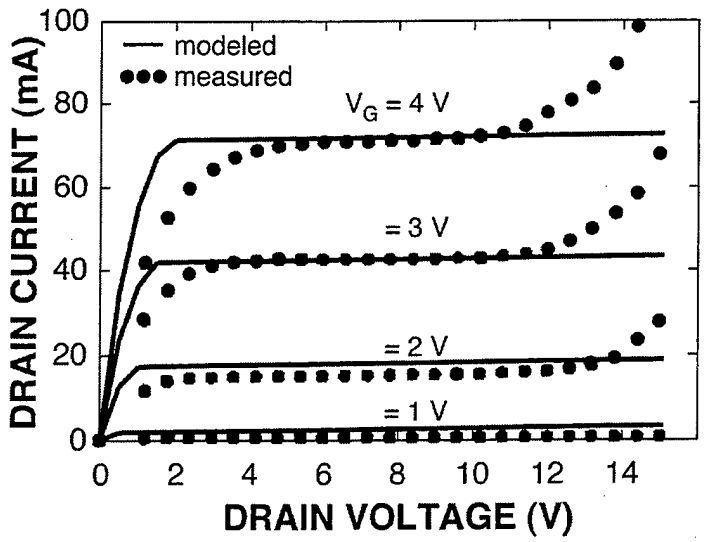


FIGURE 7.2 Measured and modeled I_d-V_{ds} characteristics.

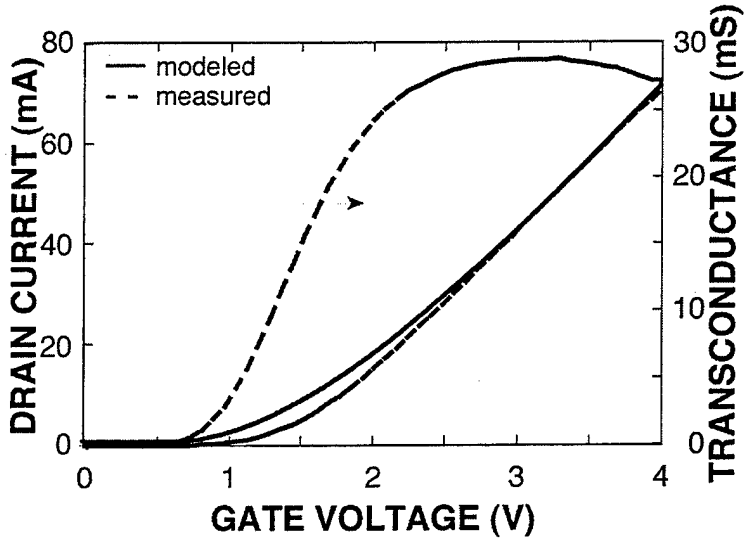


FIGURE 7.3 Measured and modeled I_d-V_{gs} and g_m-V_{gs} characteristics.

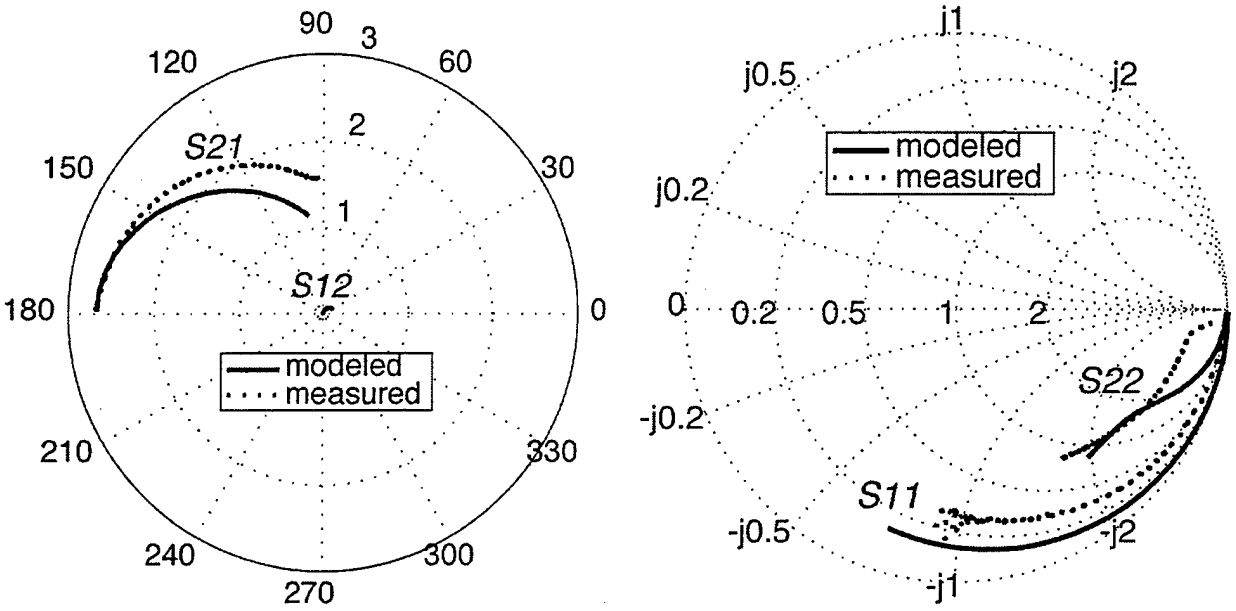


FIGURE 7.4 Measured and modeled characteristics for (a) S_{21} and S_{12} and (b) S_{11} and S_{22}.

8 CONCLUSIONS

A 50-V RF SOI LDMOSFET was designed and fabricated on a modified 1.2-μm SOI CMOS process. Measurements were performed at the wafer and package levels. Device characteristics were comparable to those of equivalent bulk RF LDMOSFETs. Model parameter extraction was also performed. It was observed that compared to the circuit model employed for bulk LDMOSFETs, it is necessary to include an additional capacitance to account for the buried oxide.

Several publications have been derived from this work. Citations are listed below.

9 REFERENCES

[1] I. Yoshida, "2-GHz Si Power MOSFET Technology," in *IEEE IEDM Tech. Dig.*, 1997, pp. 51-54.

[2] N. Camilleri, J. Costa, D. Lovelace, and D. Ngo, "Silicon MOSFETs: The Microwave Technology for the 90s," in *IEEE MTT-S Dig.*, 1993, pp. 545-548.

[3] C. Dragon, J. Costa, D. Lamey, D. Ngo, and W. Burger, "A Silicon MOS Process for Integrated Power Amplifiers," in *Proc. IEEE Microwave and Millimeter Wave Monolithic Circuits Symp.*, 1996, pp.-189-192.

[4] K. Shenai, "Optimally Scaled Low-Voltage Vertical Power DMOSFETs for High-Frequency Power Switching Applications," *IEEE Trans. Electron Devices*, vol. 37, no. 4, pp. 1141-1153, 1990.

[5] C. Hu, M.-H. Chi, and V. M. Patel, "Optimum Design of Power MOSFETs," *IEEE Trans. Electron Devices*, vol. 31, no. 12, pp. 1693-1700, 1984.

[6] G. M. Dolny, A. C. Ipri, and M. Batty, "CMOS/DMOS Power IC Technology on Thin-Film SOI Substrates," in *Proc. IEEE Int. SOI Conf.*, 1993, pp. 98-99.

[7] Y. Suzuki, T. Kishida, H. Takano, and Y. Shirai, "3-D Effect of Cell Designs on the Breakdown Voltage of Power SOI-LDMOS," in *Proc. IEEE Int. SOI Conf.*, 1996, pp. 134-135.

[8] A. Hurrich, P. Hubler, D. Eggert, and H. Kuck, "SOI-CMOS Technology with Monolithically Integrated Active and Passive RF Devices on High Resistivity SIMOX Substrates," in *Proc. IEEE Int. SOI Conf.*, 1996, pp. 130-131.

[9] M. Stuber, M. Megahed, J. J. Lee, and T. Kobayashi, "SOI CMOS with High-Performance Passive Components for Analog, RF, and Mixed-Signal Design," in *Proc. IEEE Int. SOI Conf.*, 1998, pp. 99-100.

[10] H. Neubrand, R. Constapel, M. Fuellmann, and R. Boot, "Thermal Behavior of Lateral Power Devices on SOI Substrates," in *Proc. IEEE Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 1994, pp. 123-130.

[11] E. Arnold, S. Merchant, T. Letavic, and H. Bhimnathwala, "High-Temperature Performance of SOI and Bulk-Silicon Resurf LDMOS Transistors," in *Proc. IEEE Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 1996, pp. 93-96.

[12] J. C. Tsang, J. B. McKitterick, J. A. Zolnier, and J. M. O'Connor, "A 90-V Breakdown High Temperature SOI Lateral Power nMOSFET," in *Proc. IEEE Int. Conf. High-Temperature Electronics*, 1998, pp. 215-218.

[13] J. P. Raskin, J. P. Eggermont, D. Vanhoenacker, and J. P. Colinge, "Synthetic Microwave Inductors in SOI Technology," in *Proc. IEEE Int. SOI Conf.*, 1997, pp. 90-91.

10 PUBLICATIONS DERIVED FROM THIS PROJECT

10.1 Publications in Refereed International Journals

[1] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "Modeling and Characterization of an 80-V Silicon LDMOSFET for Emerging RFIC Applications," *IEEE Trans. Electron Devices*, vol. 45, no. 7, pp. 1468-1478, July 1998.

[2] P. Khandelwal, M. Trivedi, K. Shenai, and S. K. Leong, "Thermal and Package Performance Limitations in LDMOSFET RFIC Applications," *IEEE Trans. Microwave Theory & Techniques*, vol. 47, no. 5, pp. 575-585, May 1999.

[3] M. Trivedi, P. Khandelwal, and K. Shenai, "Performance Modeling of RF Power MOSFETs," *IEEE Trans. Electron Devices*, vol. 46, no. 8, pp. 1794-1802, August 1999.

[4] M. Trivedi, P. Khandelwal, K. Shenai, and S. K. Leong, "Design and Modeling of Bulk and SOI LDMOSFETs for RF Wireless Applications," *Solid State Electronics*, August 2000, in press.

[5] K. Shenai, E. McShane, and S. K. Leong, "Lateral RF SOI Power MOSFETs with f_T of 6.9 GHz," to appear in *IEEE Electron Device Lett.*, October 2000, in press.

[6] M. Trivedi, K. Shenai, and S. K. Leong, "Comparison of VDMOSFET and LDMOSFET for Application in RF Power Amplifiers," submitted to *IEEE Trans. Microwave Theory & Techniques*, March 2000.

[7] E. McShane and K. Shenai, "The Design, Characterization, and Modeling of RF SOI LDMOSFETs on Silicon-on-Insulator Material," submitted to *IEEE Trans. Electron Devices*, August 2000.

[8] E. McShane and K. Shenai, "A Comparison of Performance of Bulk and SOI RF LDMOSFETs for Power Amplifier Applications," submitted to *IEEE Trans. Microwave Theory & Techniques*, August 2000.

10.2 Publications in International Conference Proceedings

[1] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "Modeling and Characterization of 80-V LDMOSFET for RF Communications," in *IEEE BCTM Tech. Dig.*, 1997, pp. 92-95.

[2] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "Performance Evaluation of Bulk Si and SOI RF LDMOSFETs for Emerging RFIC Applications," in *Dig. IEEE Int. SOI Conf.*, 1997, pp. 108-109.

[3] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "High-Temperature Performance of LDMOSFETs Used in RFIC Applications," Conference on *High Temperature Electronic Materials, Devices, and Sensors (HTEM)*, 1998, pp. 100-104.

[4] P. Khandelwal, M. Trivedi and K. Shenai, "Thermal Issues in LDMOSFET Packages," in *Dig. IEEE European Solid-State Device Research Conference (ESSDERC)*, 1998.

[5] P. Perugupalli, Y. Xu, and K. Shenai, "Measurement of Thermal and Packaging Limitations in LDMOSFETs for RFIC Applications," in *Proc. IEEE Instrumentation and Measurement Technology Conf. (IMTC)*, 1998, pp. 160-164.

[6] M. Trivedi and K. Shenai, "Comparison of RF Performance of Vertical and Lateral DMOSFET," in *Proc. IEEE Int. Symp. Power Semiconductor Devices and IC's (ISPSD)*, 1999, pp. 245-248.

[7] E. McShane and K. Shenai, "Microwave Performance of Power MOSFETs on SOI Substrates," to be presented at *IEEE Cornell Conf. Advanced Concepts in High Performance Devices*, 2000.

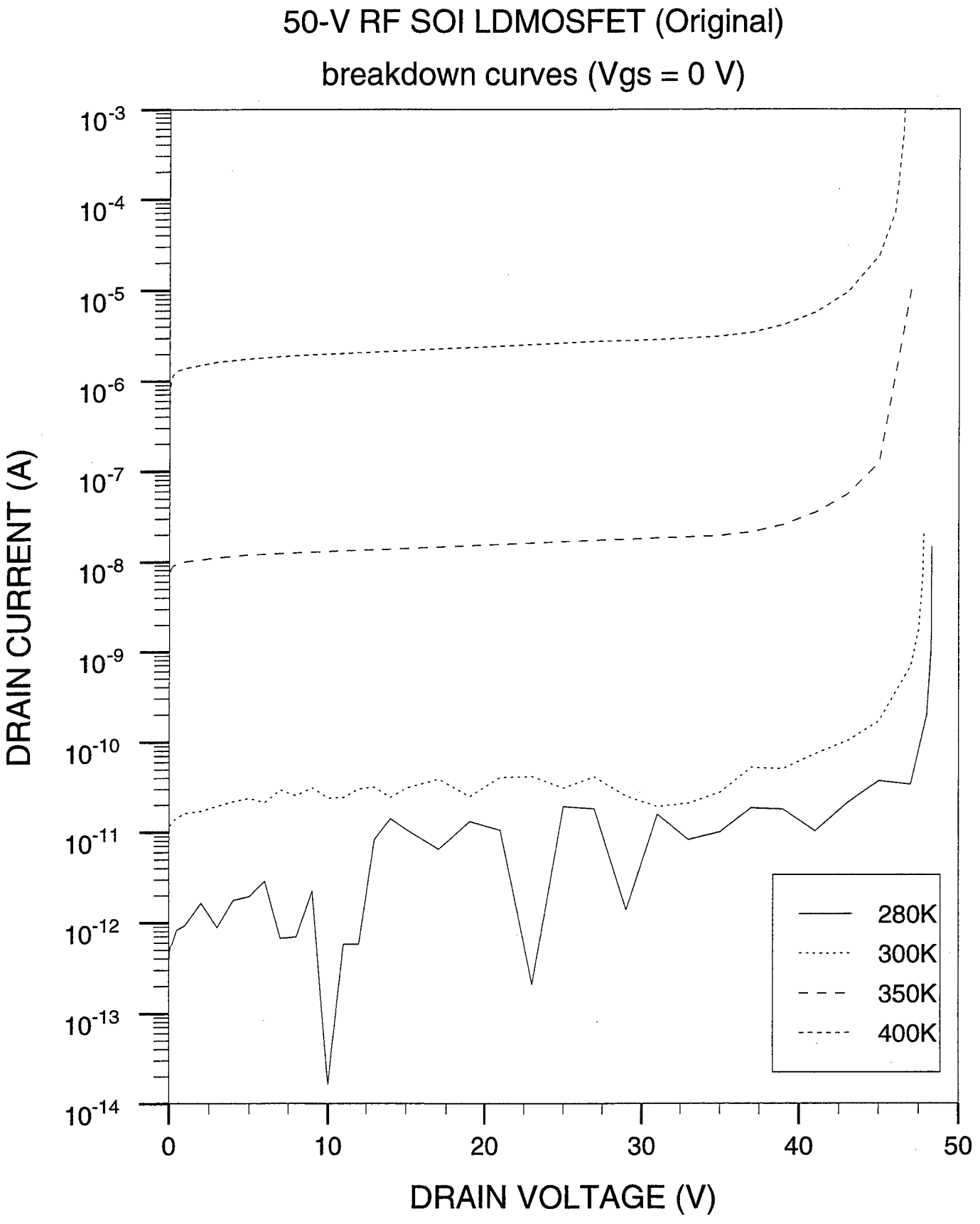
[8] E. McShane and K. Shenai, "SOI Power MOSFETs for RF Wireless Communications," to be presented at *Int. Conf. Microelectronics and Packaging (SBMicro)*, 2000.

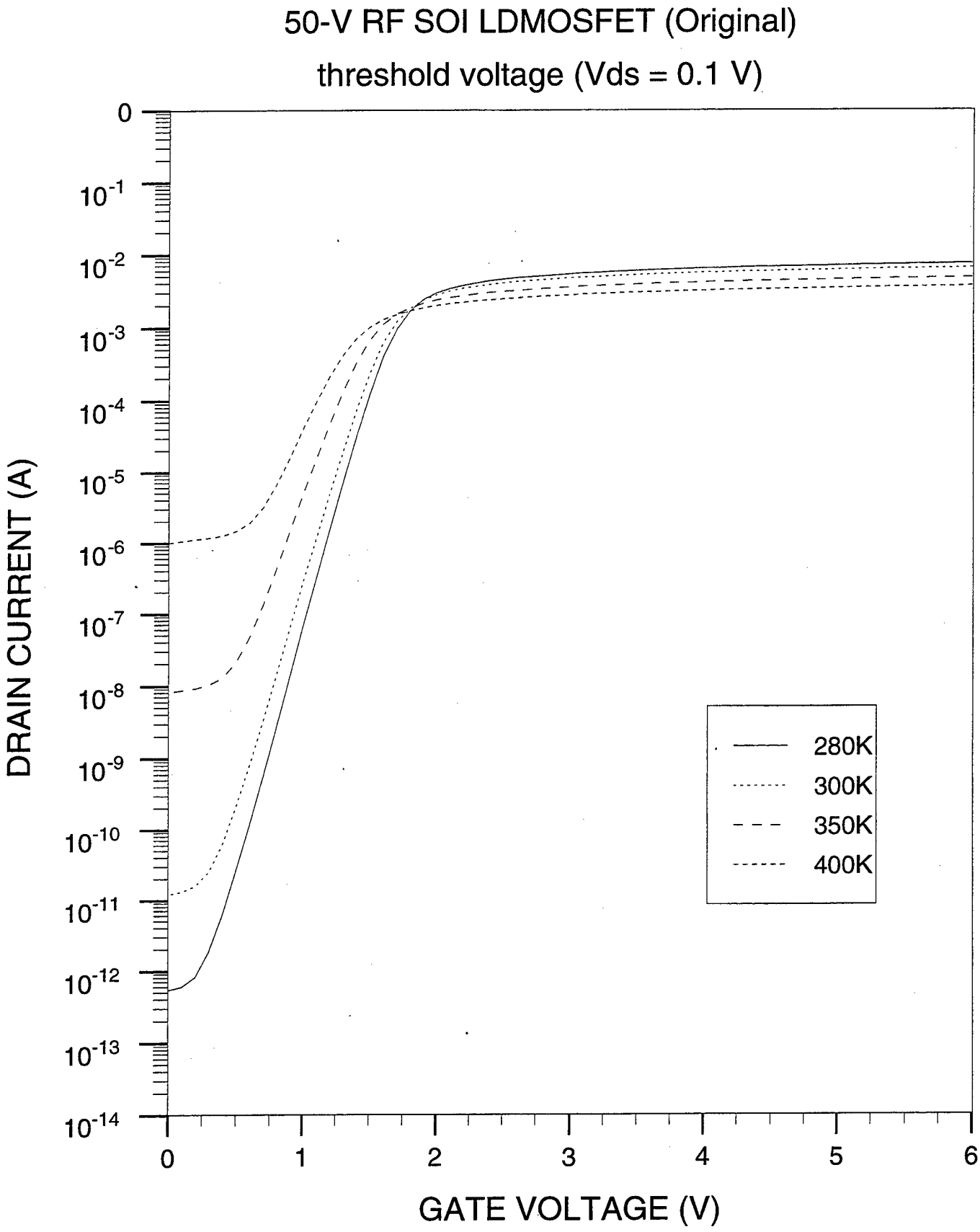
APPENDIX A

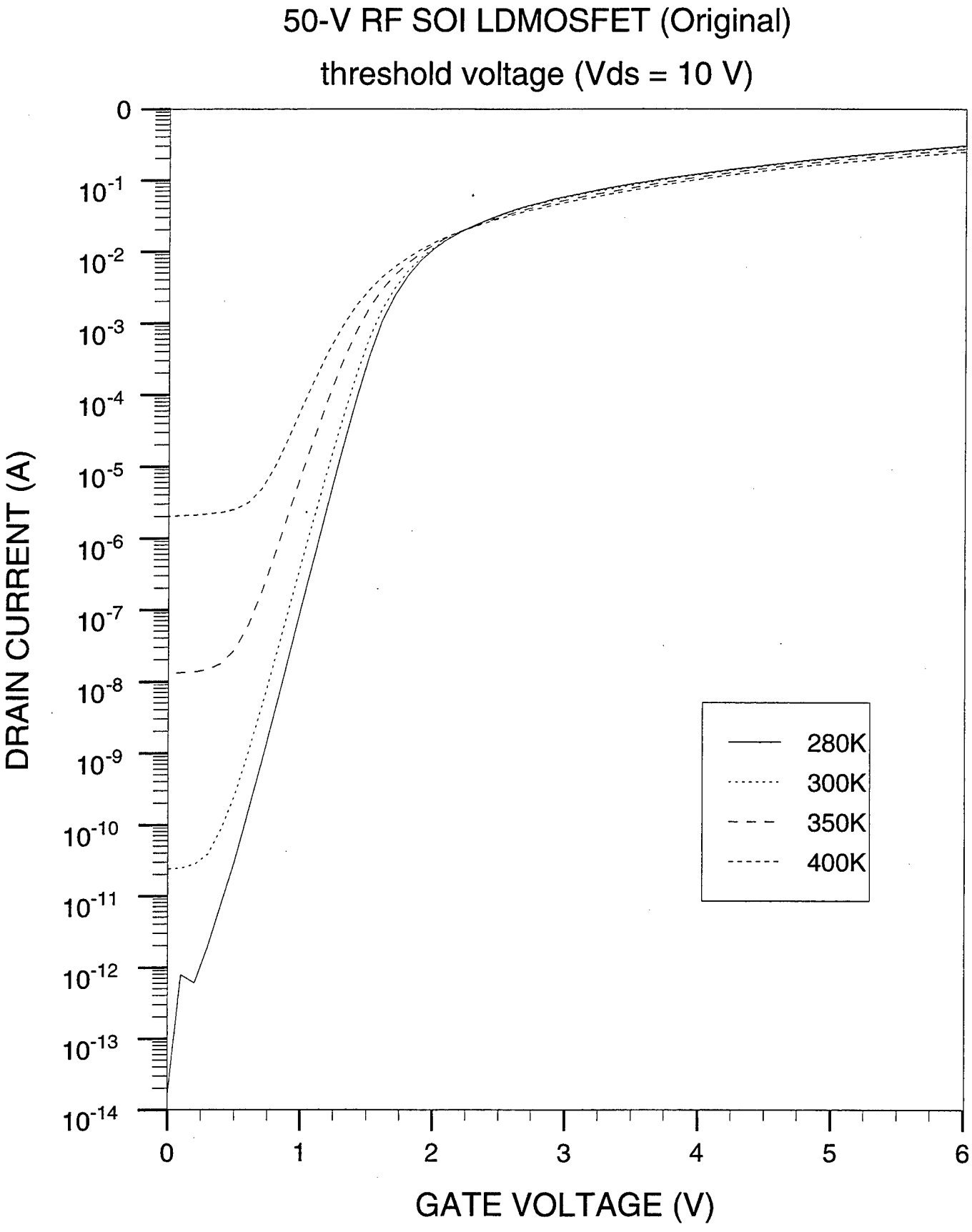
Simulation Data: Initial 2-D Numerical Results of Process and Device Design

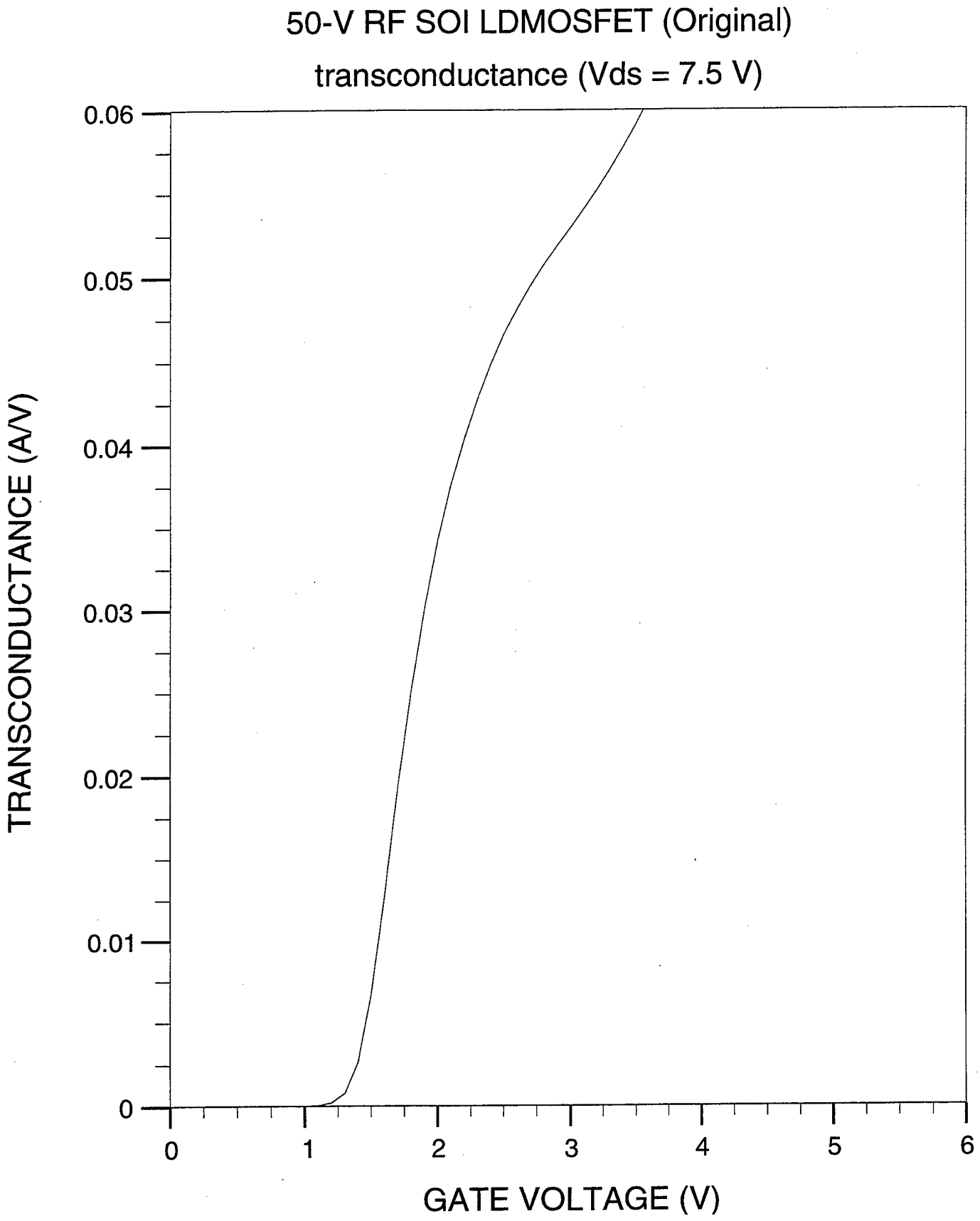
The contents of this section consist of the following waveforms. Bias conditions are noted as appropriate. All 2-D simulations were performed for 280K, 300K, 350K, and 400K.

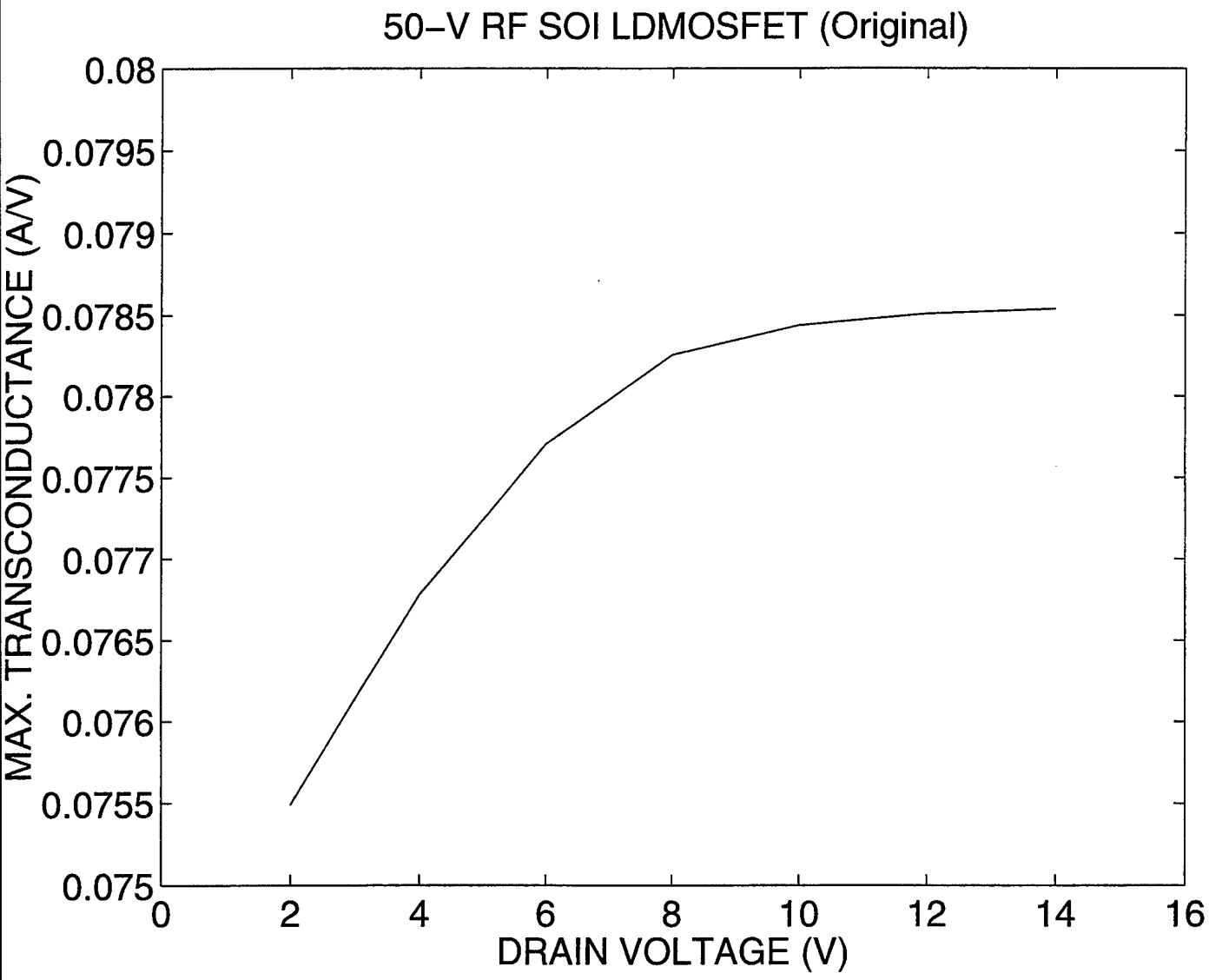
Name	**Conditions**
Drain-source static breakdown (BV_{ds})	V_{gs} = 0 V; V_{ds} = swept
Threshold voltage (V_T)	V_{ds} = 0.1,10 V; V_{gs} = 0–6 V
Transconductance versus gate bias (g_m-V_{gs})	V_{ds} = 7.5 V; V_{gs} = 0–6 V
Maximum transconductance versus drain bias ($g_{m,max}$-V_{ds})	V_{ds} = 2–14 V; V_{gs} = 0–6 V
Forward conduction (I_d-V_{ds})	V_{ds} = 0–18 V; V_{gs} = 2,3,4,5,6 V
Scattering parameters (S_{11} and S_{22})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 10 MHz – 2.9 GHz
Scattering parameters (S_{12} and S_{21})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 10 MHz – 2.9 GHz

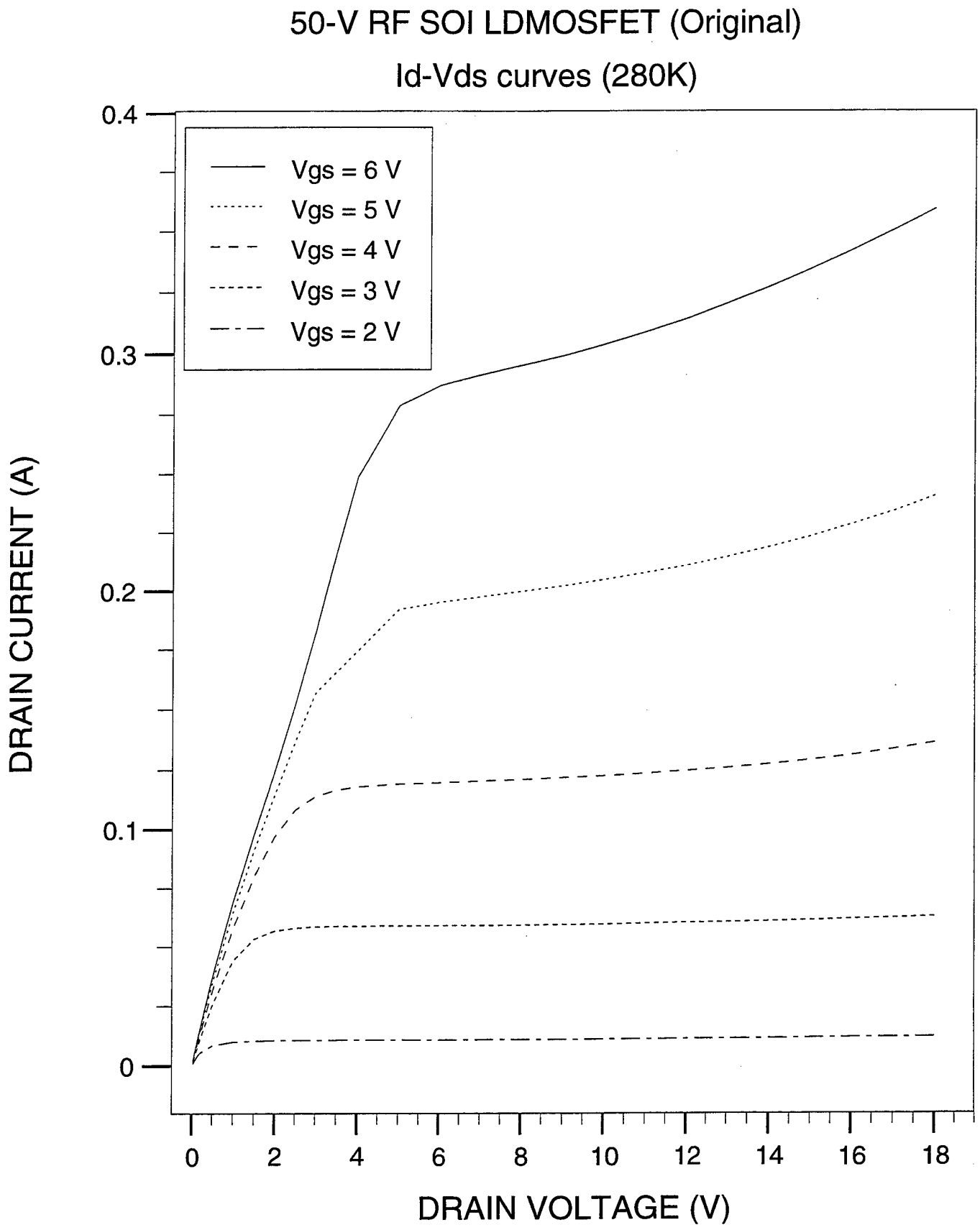

50-V RF SOI LDMOSFET (Original)
breakdown curves (Vgs = 0 V)
DRAIN CURRENT (A)
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
10-13
10-14
0
10
20
30
40
50
DRAIN VOLTAGE (V)
280K
300K
350K
400K

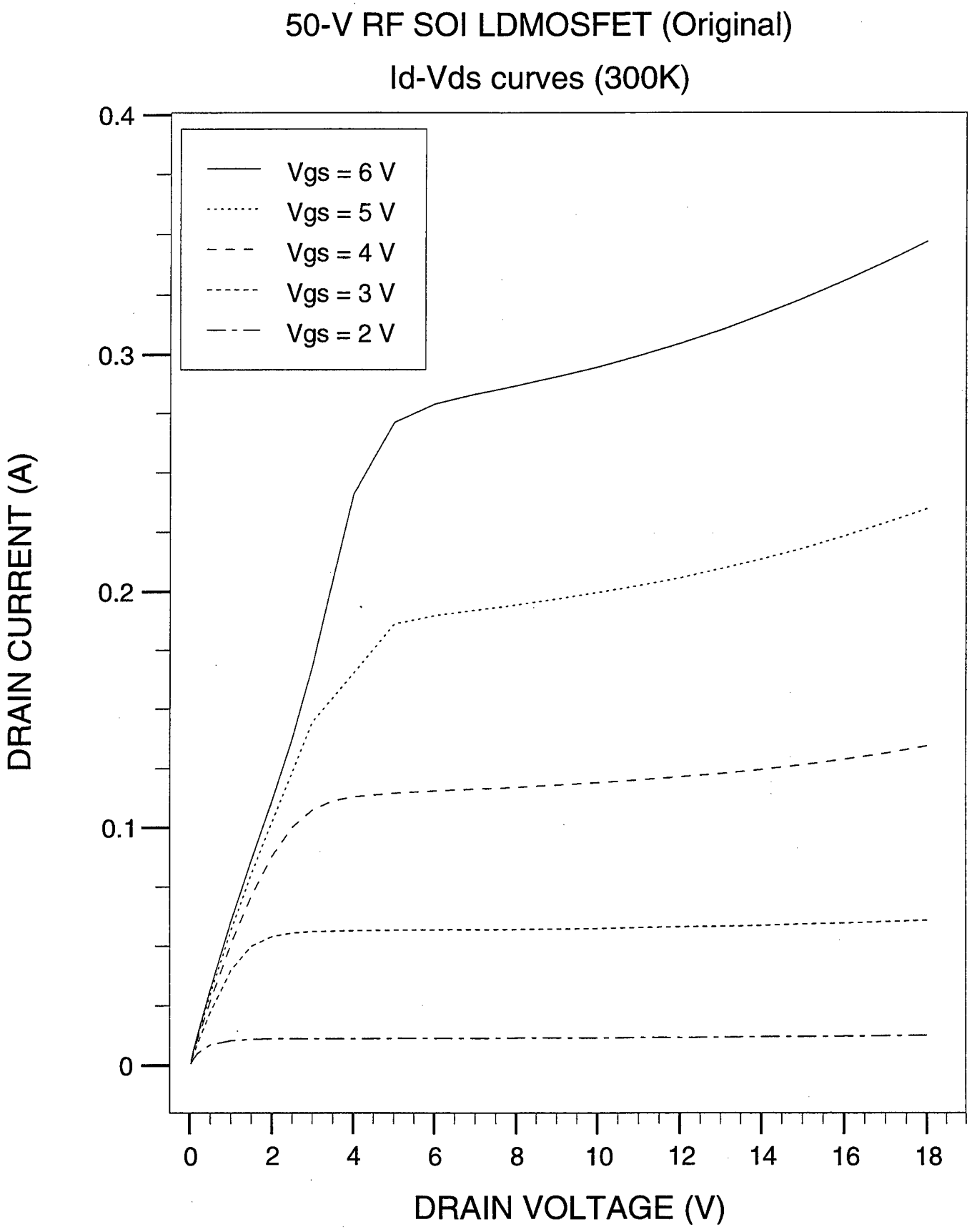

50-V RF SOI LDMOSFET (Original)
threshold voltage (Vds = 0.1 V)
DRAIN CURRENT (A)
0
10-1
10-2
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
10-13
10-14
0
1
2
3
4
5
6
GATE VOLTAGE (V)
280K
300K
350K
400K

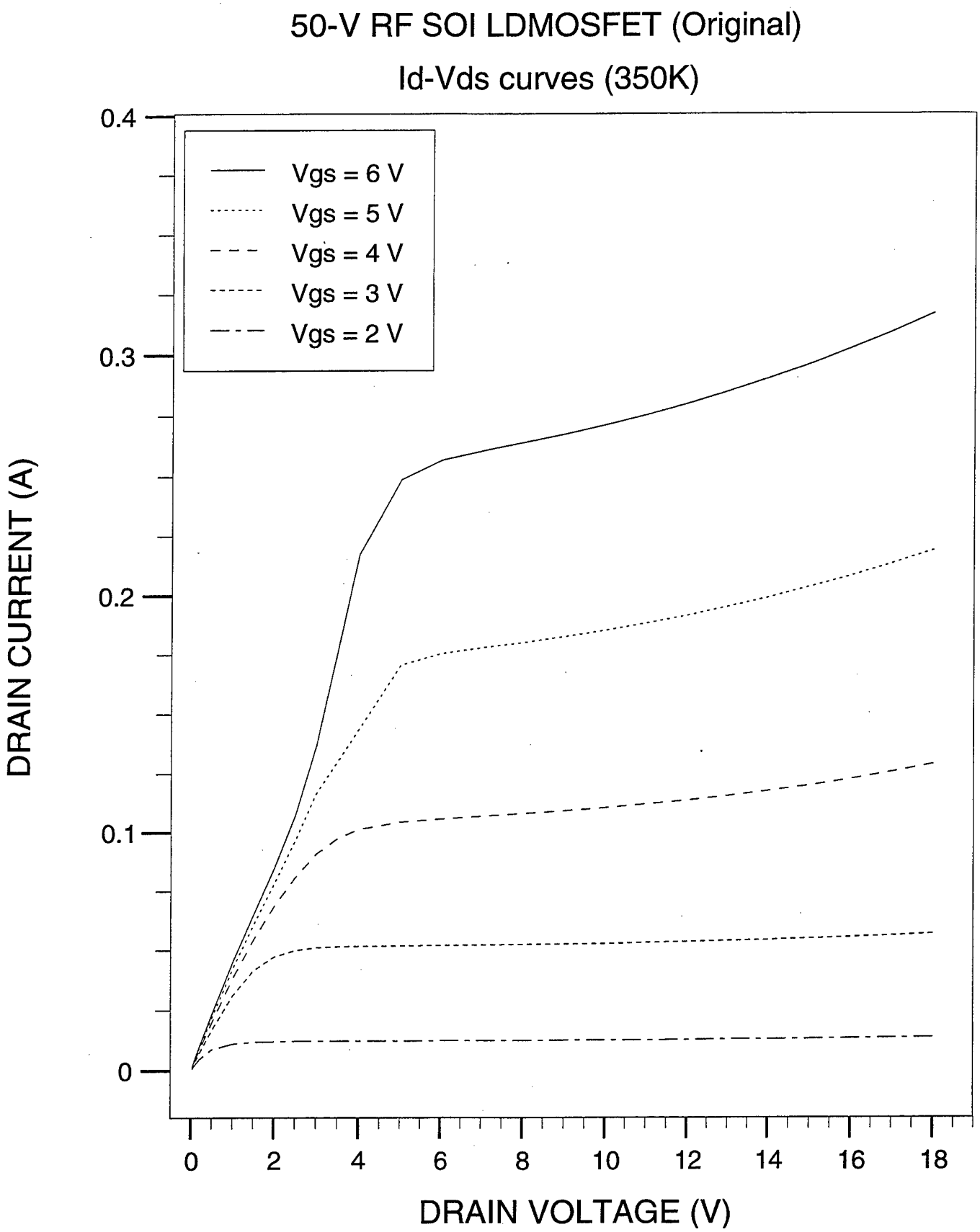

50-V RF SOI LDMOSFET (Original)
threshold voltage (Vds = 10 V)
DRAIN CURRENT (A)
0
10-1
10-2
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
10-13
10-14
0
1
2
3
4
5
6
GATE VOLTAGE (V)
280K
300K
350K
400K

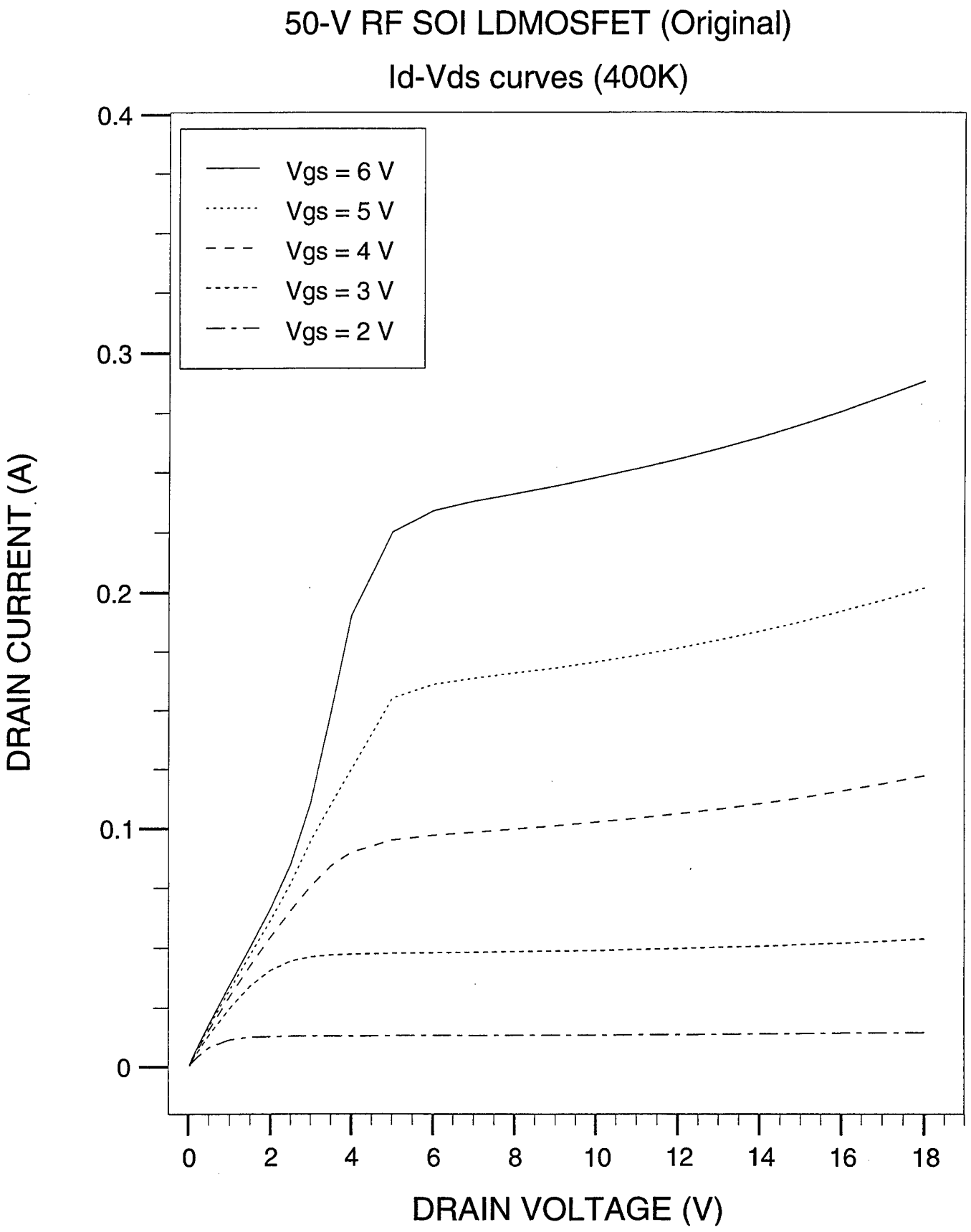

50-V RF SOI LDMOSFET (Original)
transconductance (Vds = 7.5 V)
TRANSCONDUCTANCE (A/V)
0.06
0.05
0.04
0.03
0.02
0.01
0
0
1
2
3
4
5
6
GATE VOLTAGE (V)


50–V RF SOI LDMOSFET (Original)
MAX. TRANSCONDUCTANCE (A/V)
0.08
0.0795
0.079
0.0785
0.078
0.0775
0.077
0.0765
0.076
0.0755
0.075
0
2
4
6
8
10
12
14
16
DRAIN VOLTAGE (V)


50-V RF SOI LDMOSFET (Original)
Id-Vds curves (280K)
Vgs = 6 V
Vgs = 5 V
Vgs = 4 V
Vgs = 3 V
Vgs = 2 V
0.4
0.3
0.2
0.1
0
DRAIN CURRENT (A)
0
2
4
6
8
10
12
14
16
18
DRAIN VOLTAGE (V)

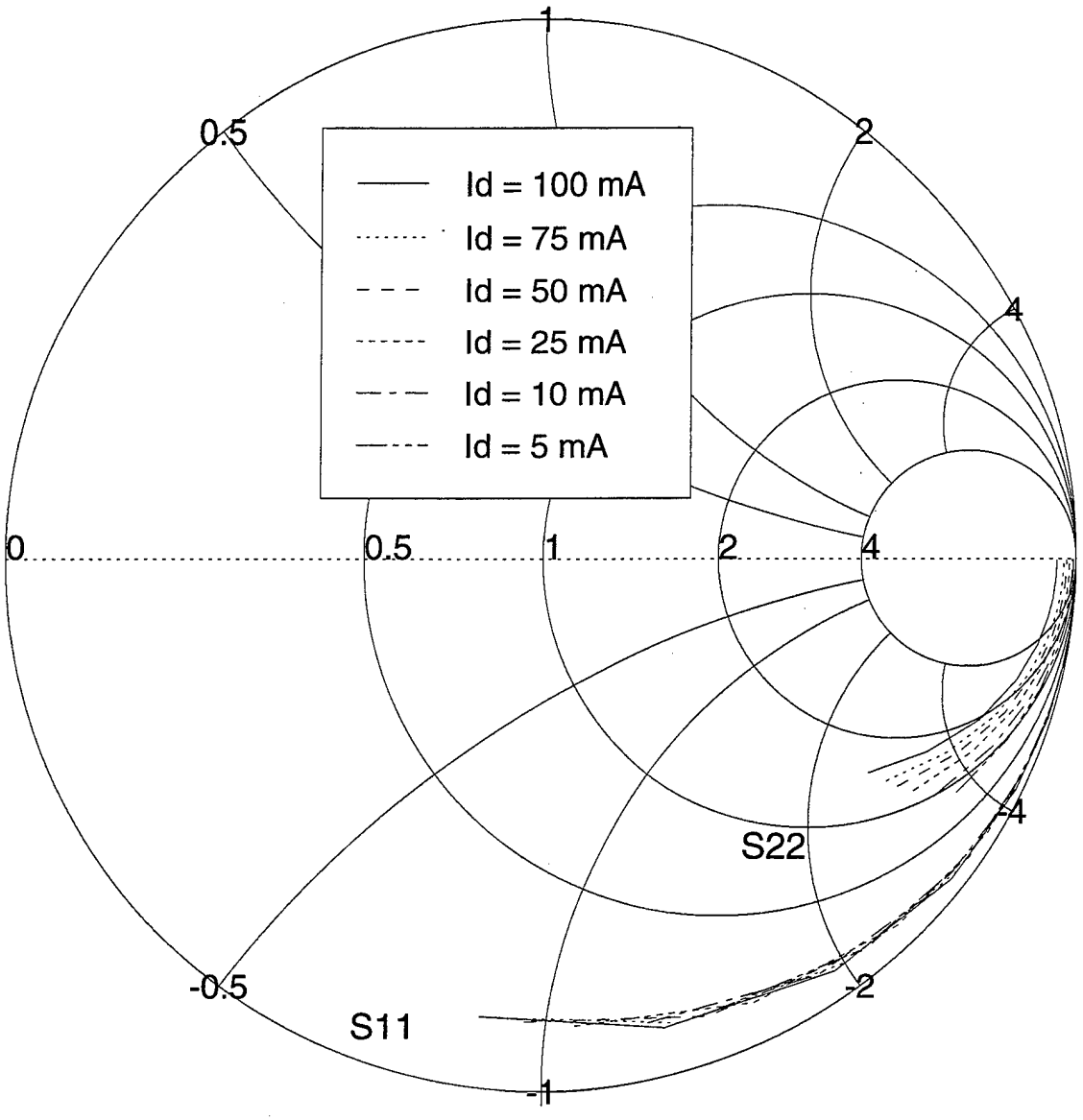

50-V RF SOI LDMOSFET (Original)
Id-Vds curves (300K)
Vgs = 6 V
Vgs = 5 V
Vgs = 4 V
Vgs = 3 V
Vgs = 2 V
0.4
0.3
0.2
0.1
0
DRAIN CURRENT (A)
0
2
4
6
8
10
12
14
16
18
DRAIN VOLTAGE (V)


50-V RF SOI LDMOSFET (Original)
Id-Vds curves (350K)
Vgs = 6 V
Vgs = 5 V
Vgs = 4 V
Vgs = 3 V
Vgs = 2 V
DRAIN CURRENT (A)
0.4
0.3
0.2
0.1
0
0
2
4
6
8
10
12
14
16
18
DRAIN VOLTAGE (V)


50-V RF SOI LDMOSFET (Original)
Id-Vds curves (400K)
Vgs = 6 V
Vgs = 5 V
Vgs = 4 V
Vgs = 3 V
Vgs = 2 V
0.4
0.3
0.2
0.1
0
DRAIN CURRENT (A)
0
2
4
6
8
10
12
14
16
18
DRAIN VOLTAGE (V)

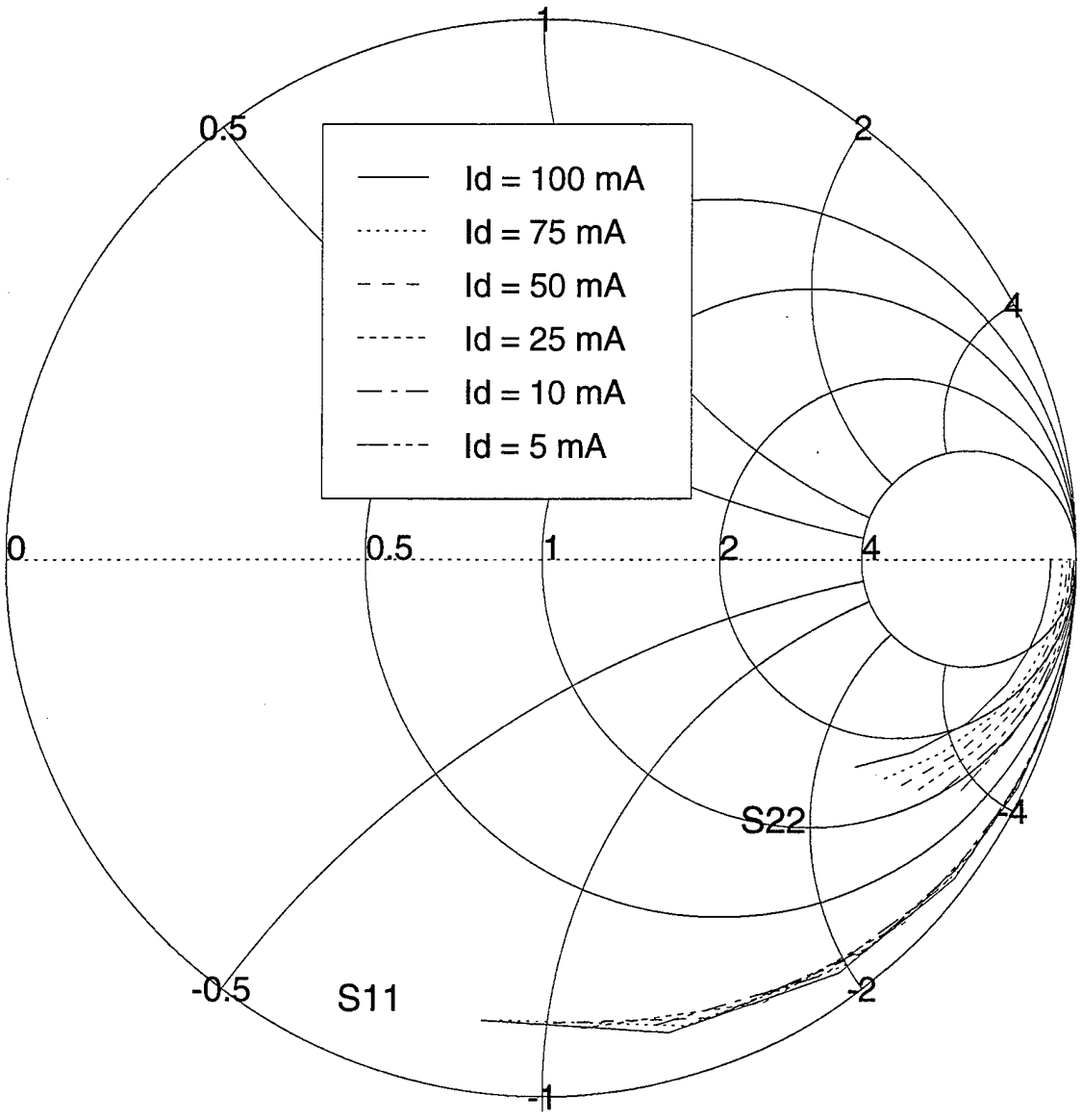
50-V RF SOI LDMOSFET (Original)

S11 and S22 (280K)



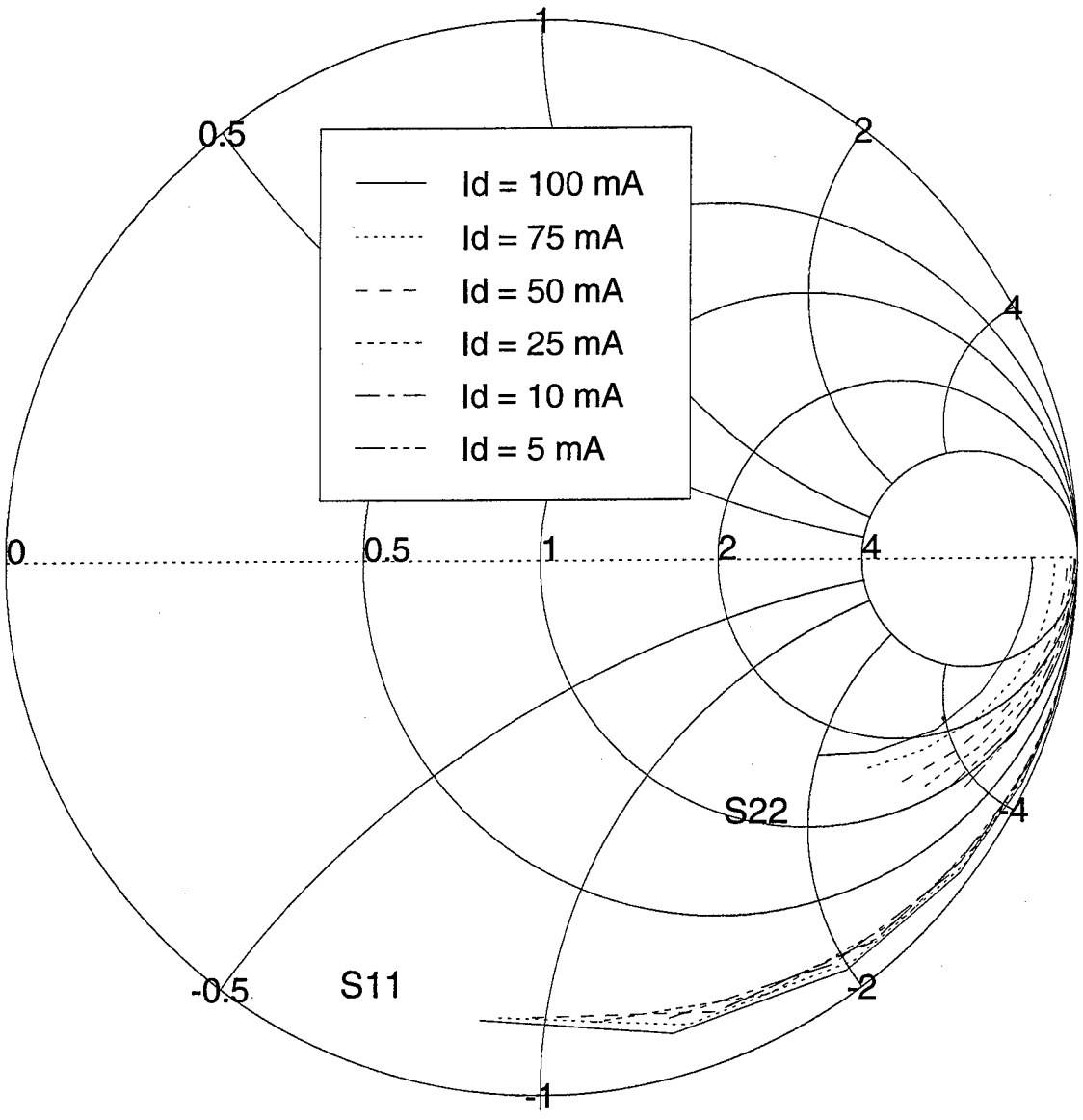
50-V RF SOI LDMOSFET (Original)

S11 and S22 (300K)



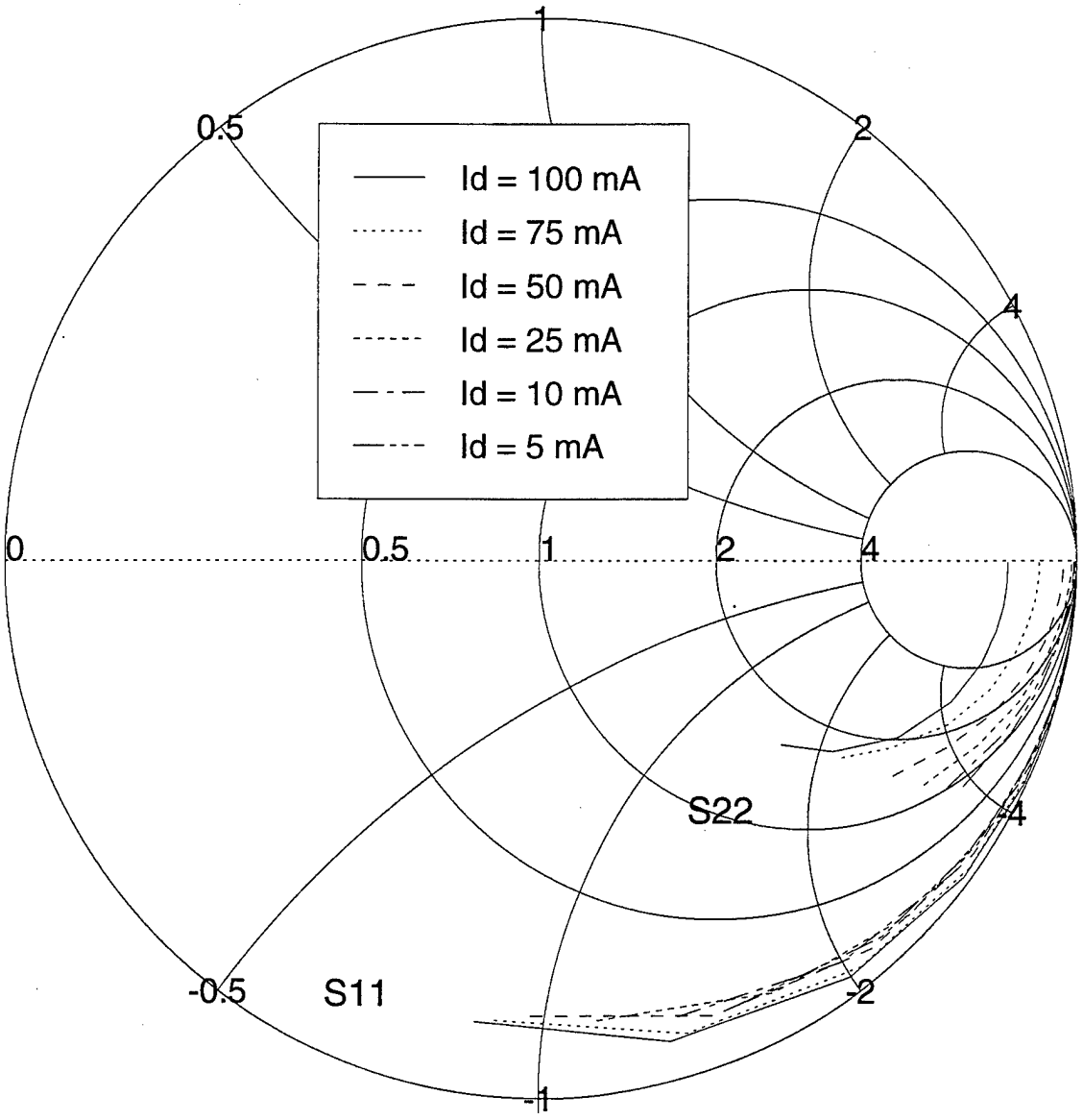
50-V RF SOI LDMOSFET (Original)

S11 and S22 (350K)



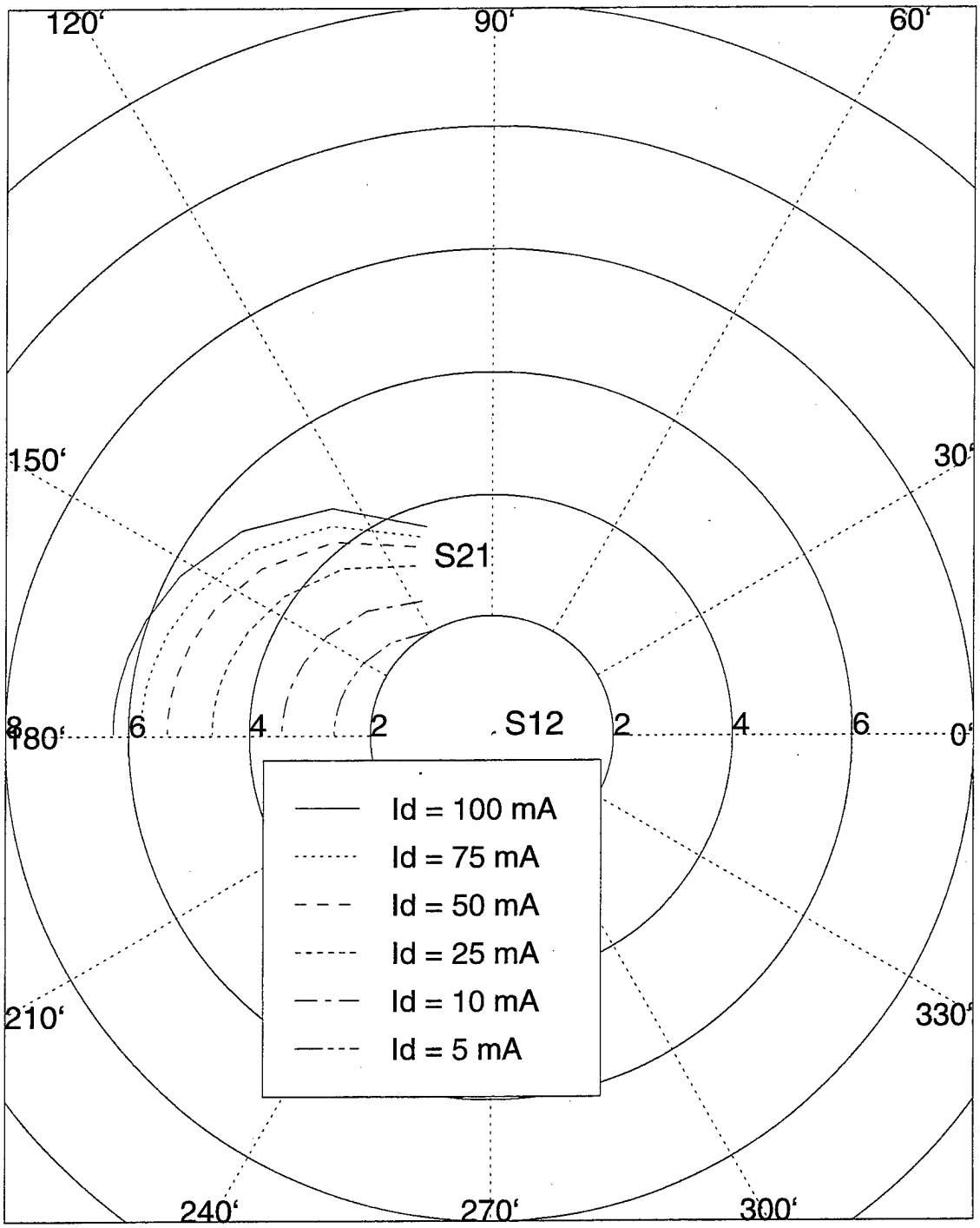
50-V RF SOI LDMOSFET (Original)

S11 and S22 (400K)



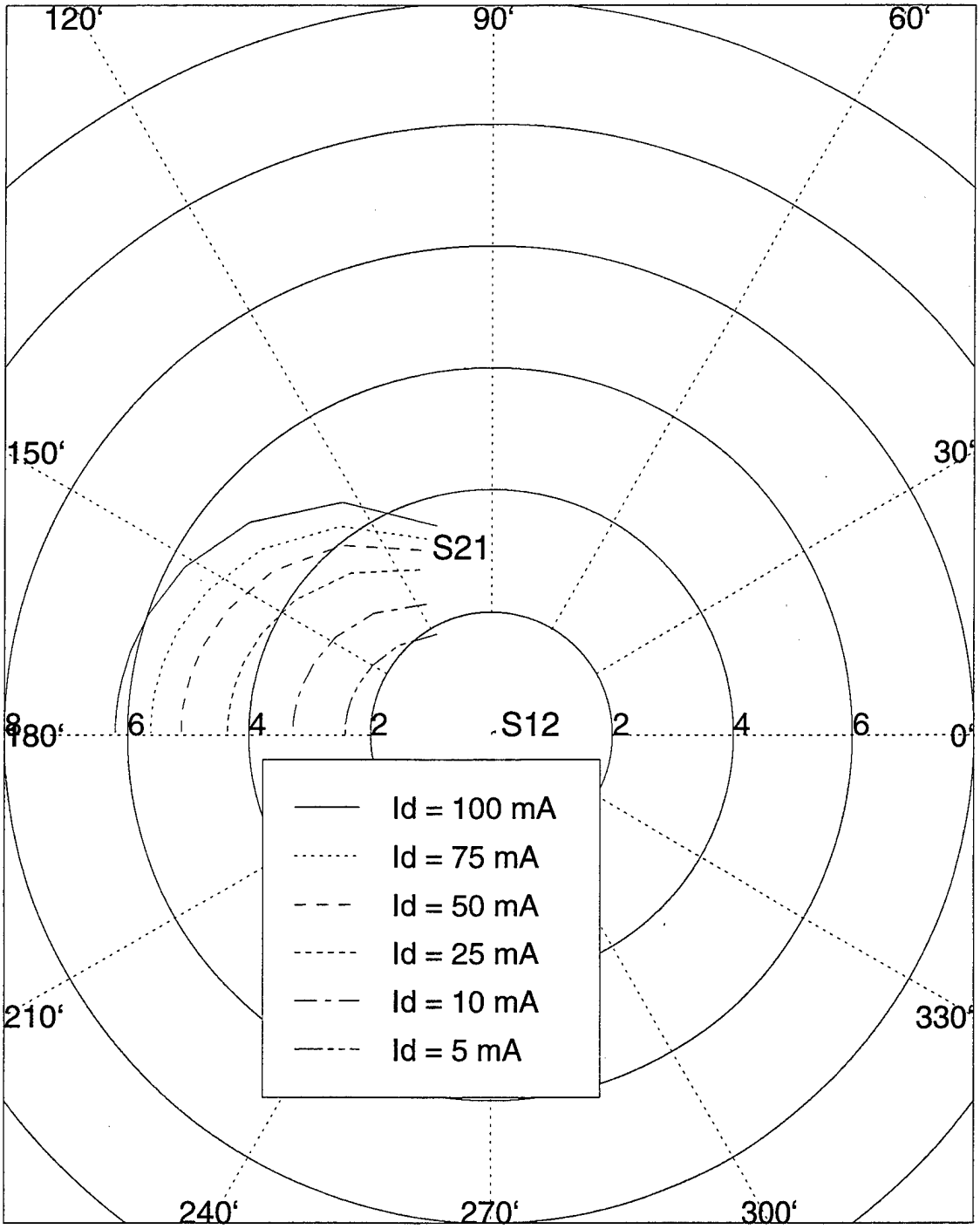
50-V RF SOI LDMOSFET (Original)

S12 and S21 (280K)



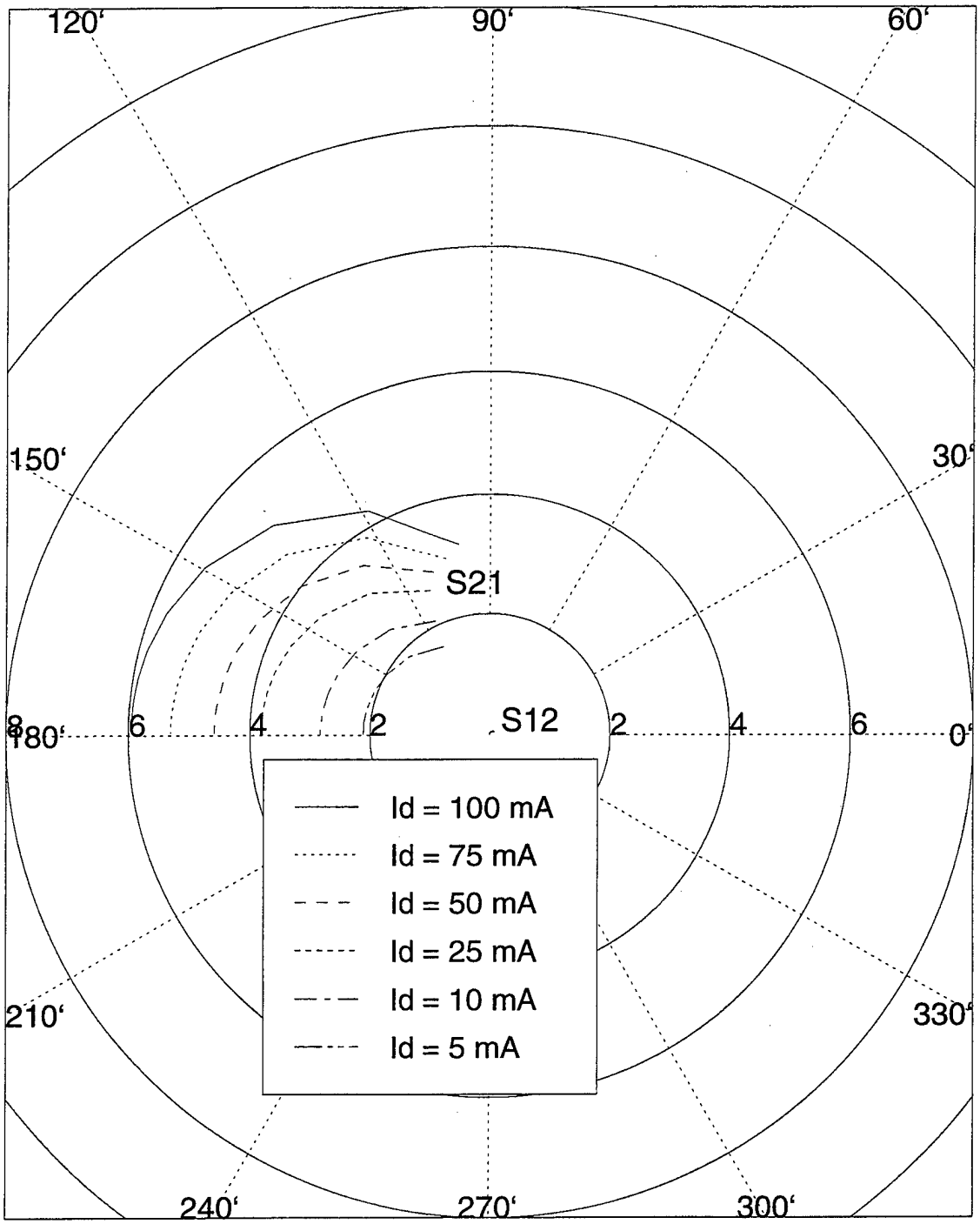
50-V RF SOI LDMOSFET (Original)

S12 and S21 (300K)



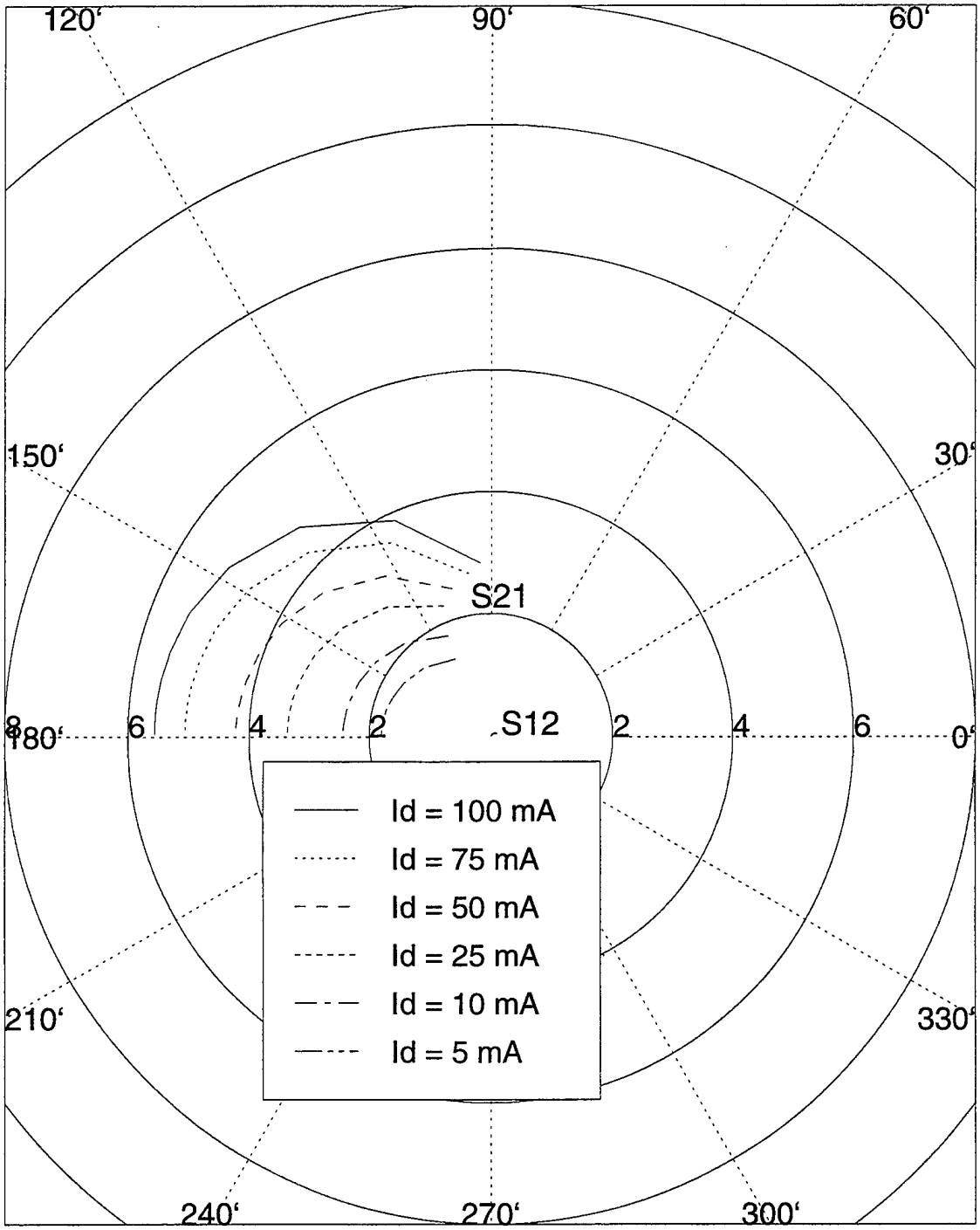
50-V RF SOI LDMOSFET (Original)

S12 and S21 (350K)



50-V RF SOI LDMOSFET (Original)

S12 and S21 (400K)

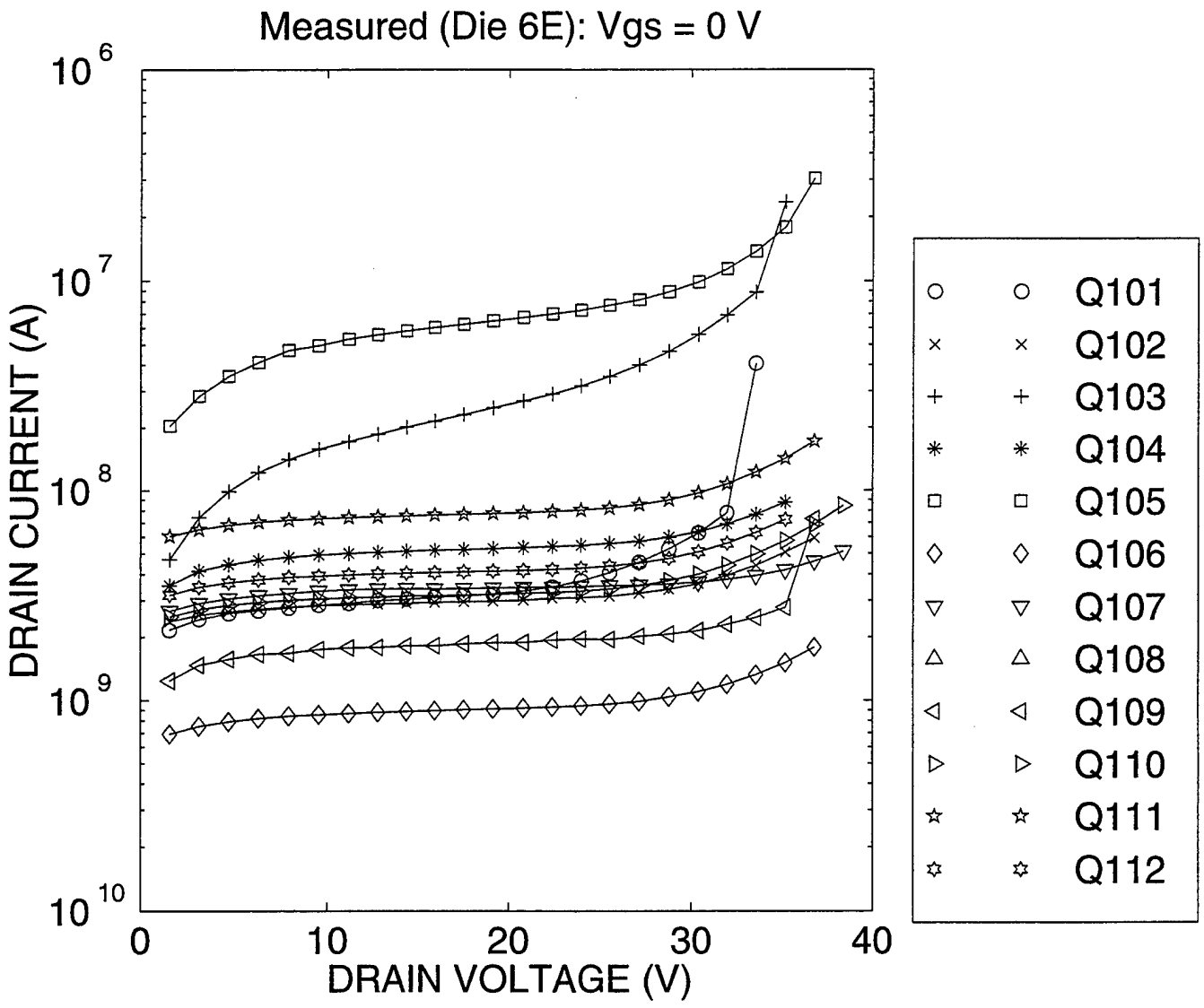


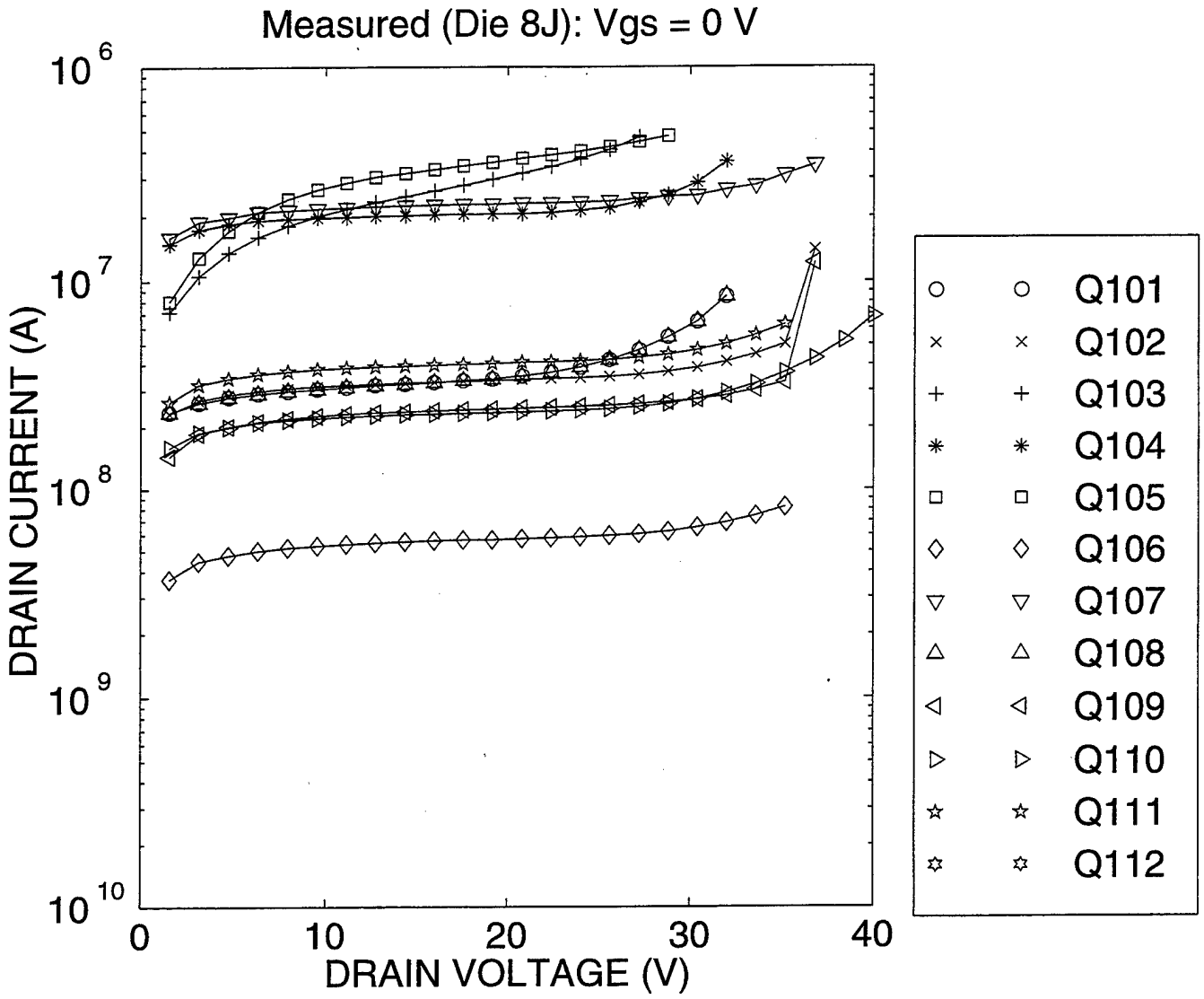
APPENDIX B

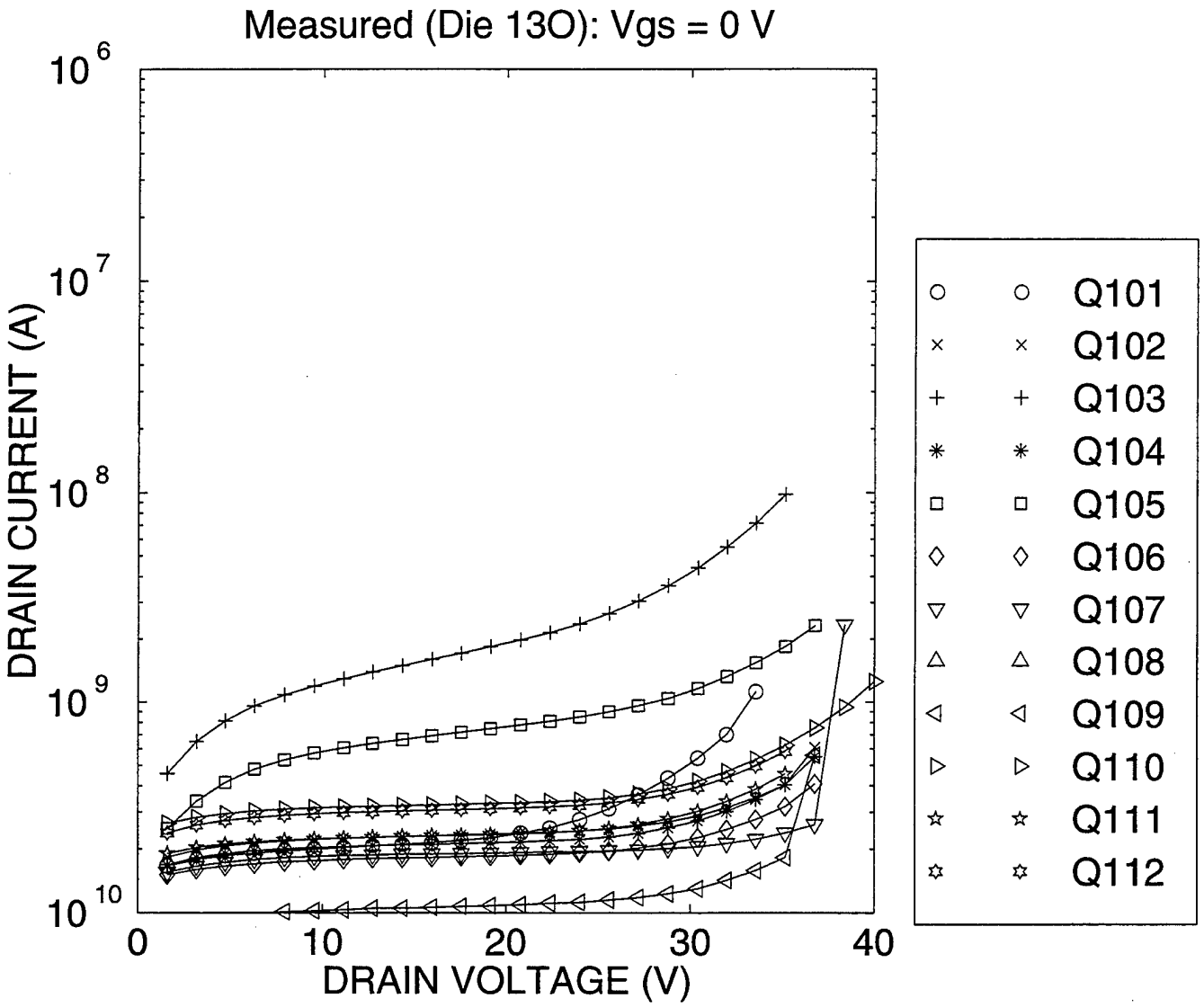
Measured Data: Fabricated 50-V RF SOI LDMOSFET Parts

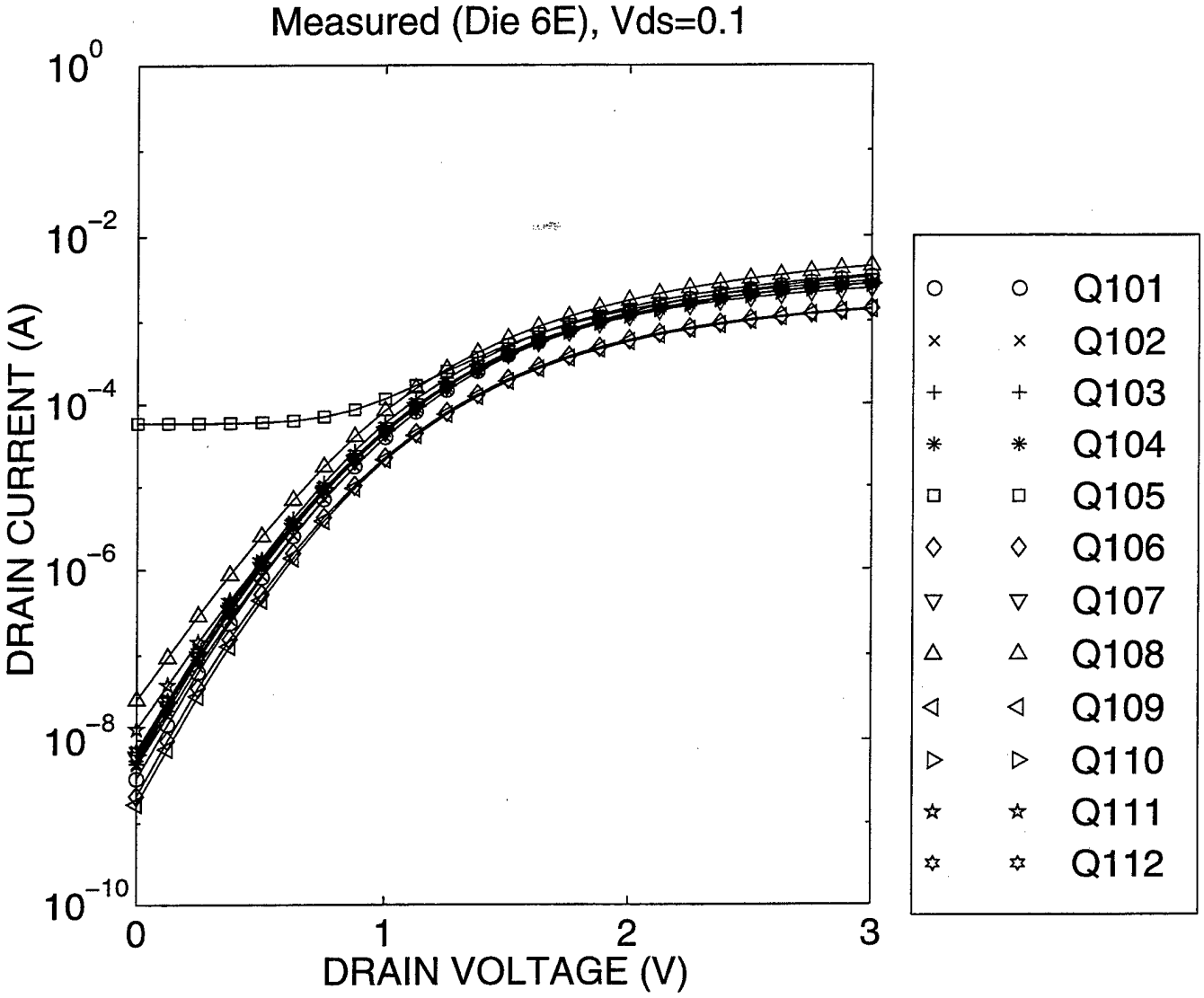
The contents of this section consist of the following waveforms. Bias conditions are noted as appropriate. All 2-D simulations were performed for 280K, 300K, 350K, and 400K.

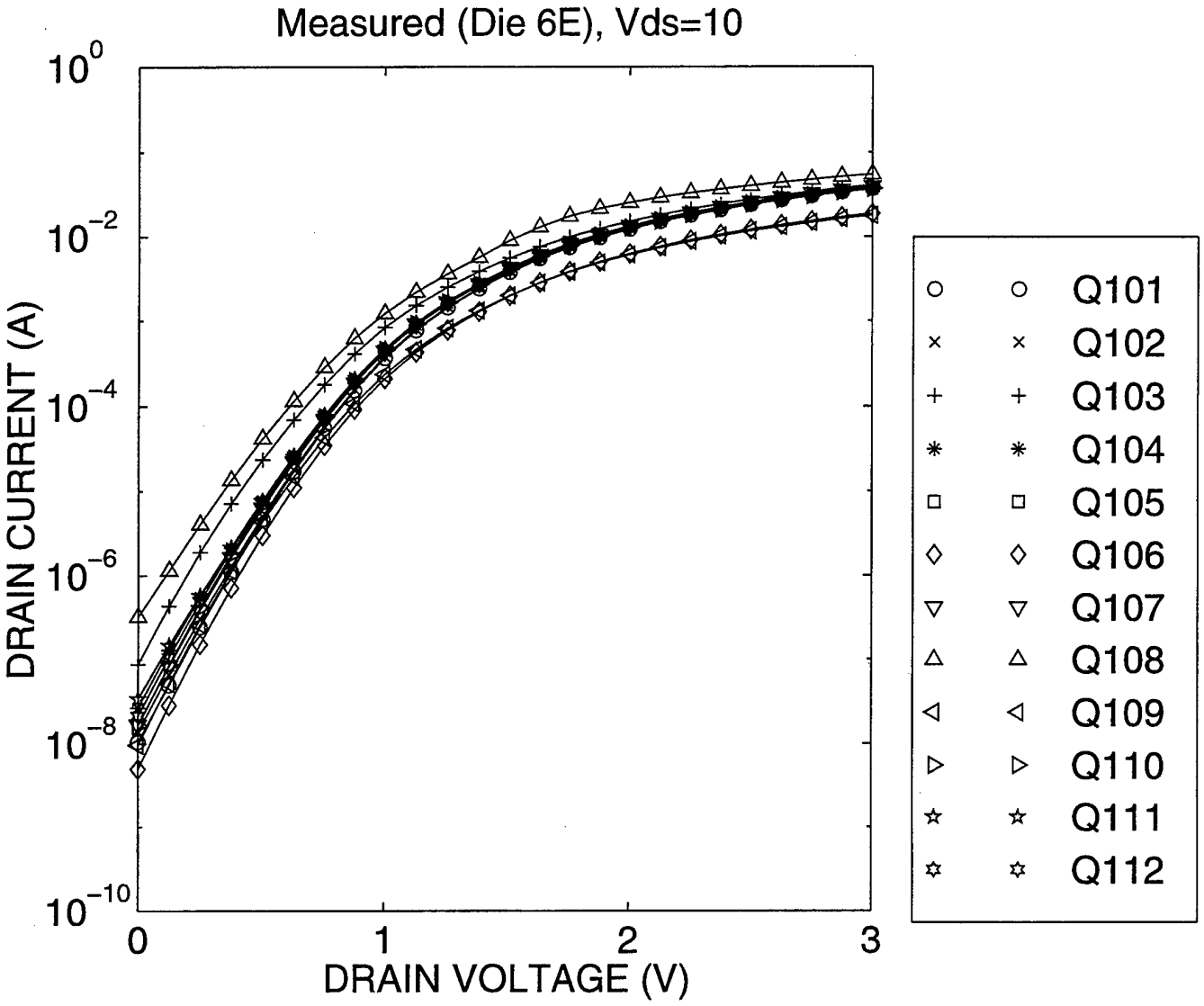
Name	**Conditions**
Drain-source static breakdown (BV_{ds})	V_{gs} = 0 V; V_{ds} = swept
Threshold voltage (V_T)	V_{ds} = 0.1,10 V; V_{gs} = 0–6 V
Transconductance versus gate bias (g_m-V_{gs})	V_{ds} = 7.5 V; V_{gs} = 0–6 V
Maximum transconductance versus drain bias ($g_{m,max}$-V_{ds})	V_{ds} = 2–14 V; V_{gs} = 0–6 V
Forward conduction (I_d-V_{ds})	V_{ds} = 0–15 V; V_{gs} = 2,3,4,5,6 V
Scattering parameters (S_{11} and S_{22})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 10 MHz – 3 GHz
Scattering parameters (S_{12} and S_{21})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 10 MHz – 3 GHz
Unity current gain frequency versus drain current (f_T-I_d)	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA

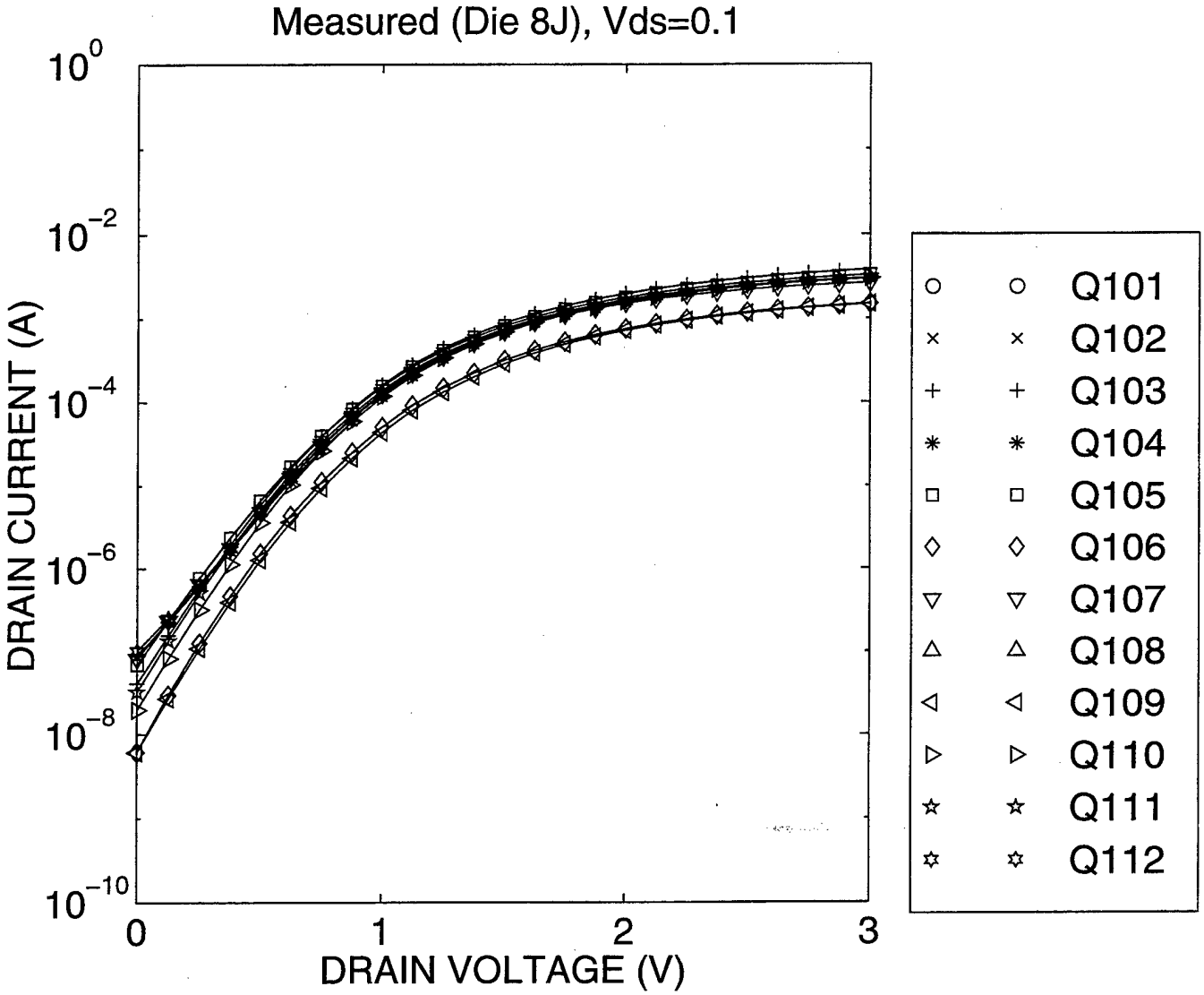

Measured (Die 6E): Vgs = 0 V
DRAIN CURRENT (A)
10 6
10 7
10 8
10 9
10 10
0
10
20
30
40
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

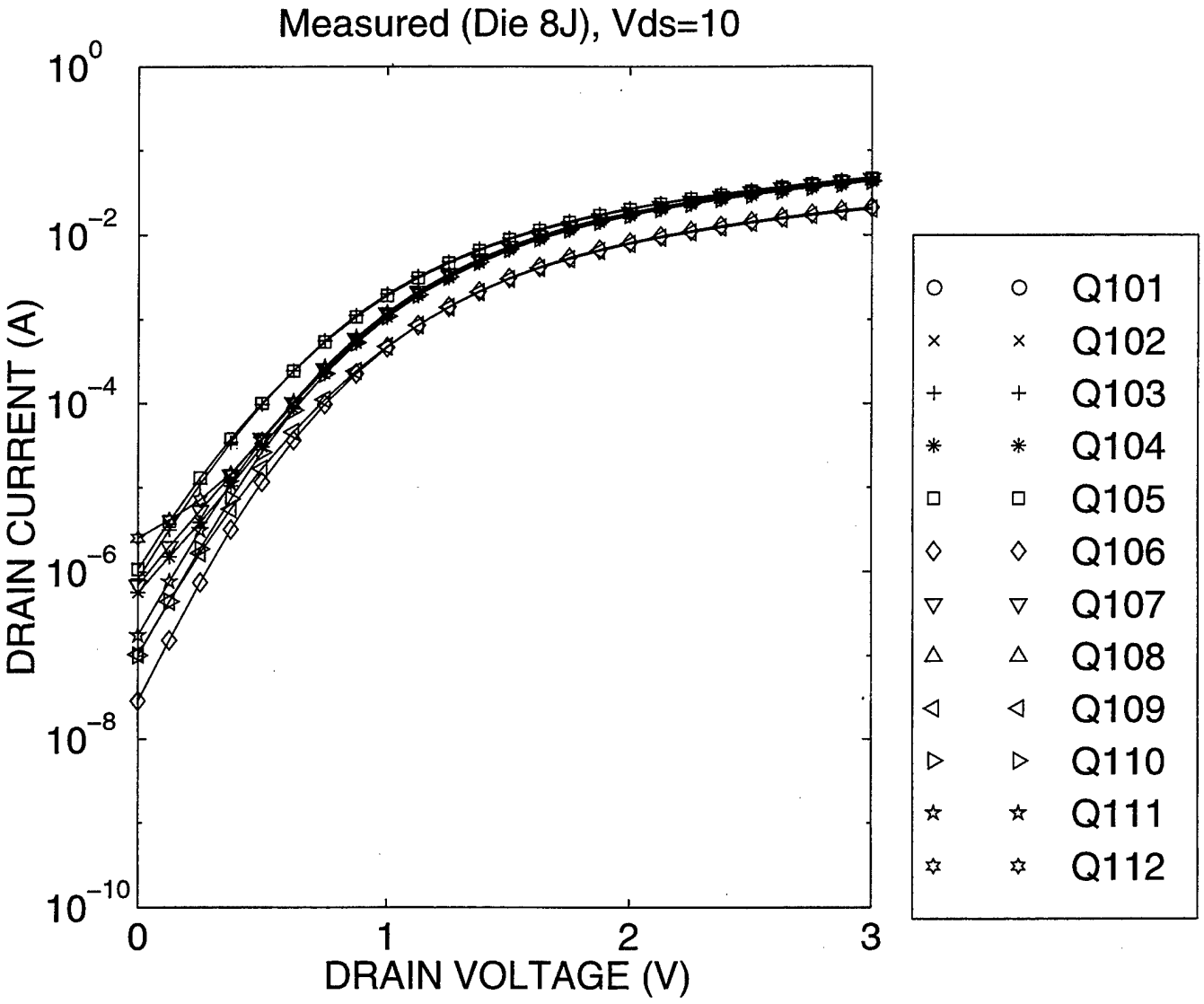

Measured (Die 8J): Vgs = 0 V
DRAIN CURRENT (A)
10^{6}
10^{7}
10^{8}
10^{9}
10^{10}
0
10
20
30
40
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

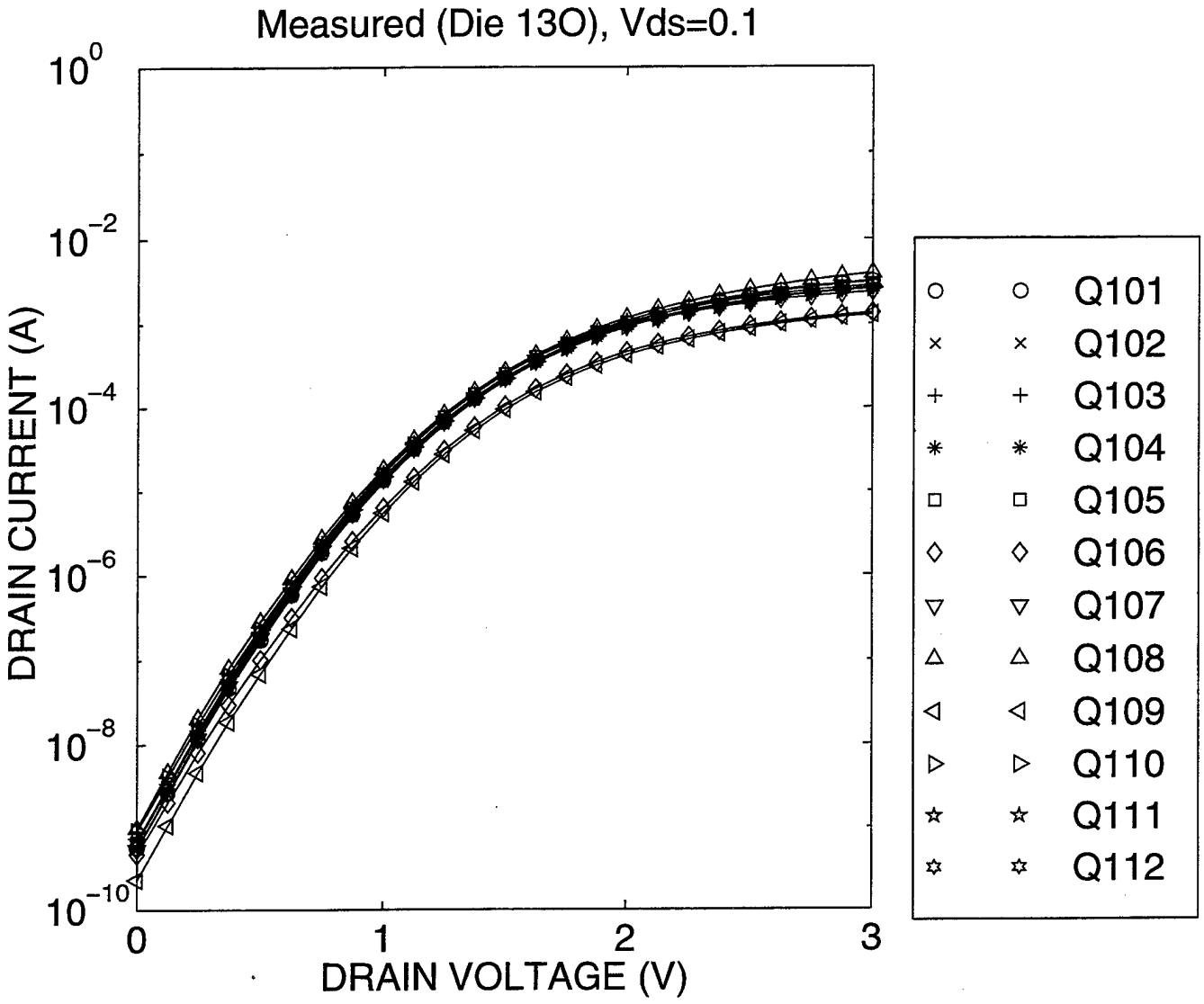

Measured (Die 13O): Vgs = 0 V
DRAIN CURRENT (A)
10^6
10^7
10^8
10^9
10^10
0
10
20
30
40
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

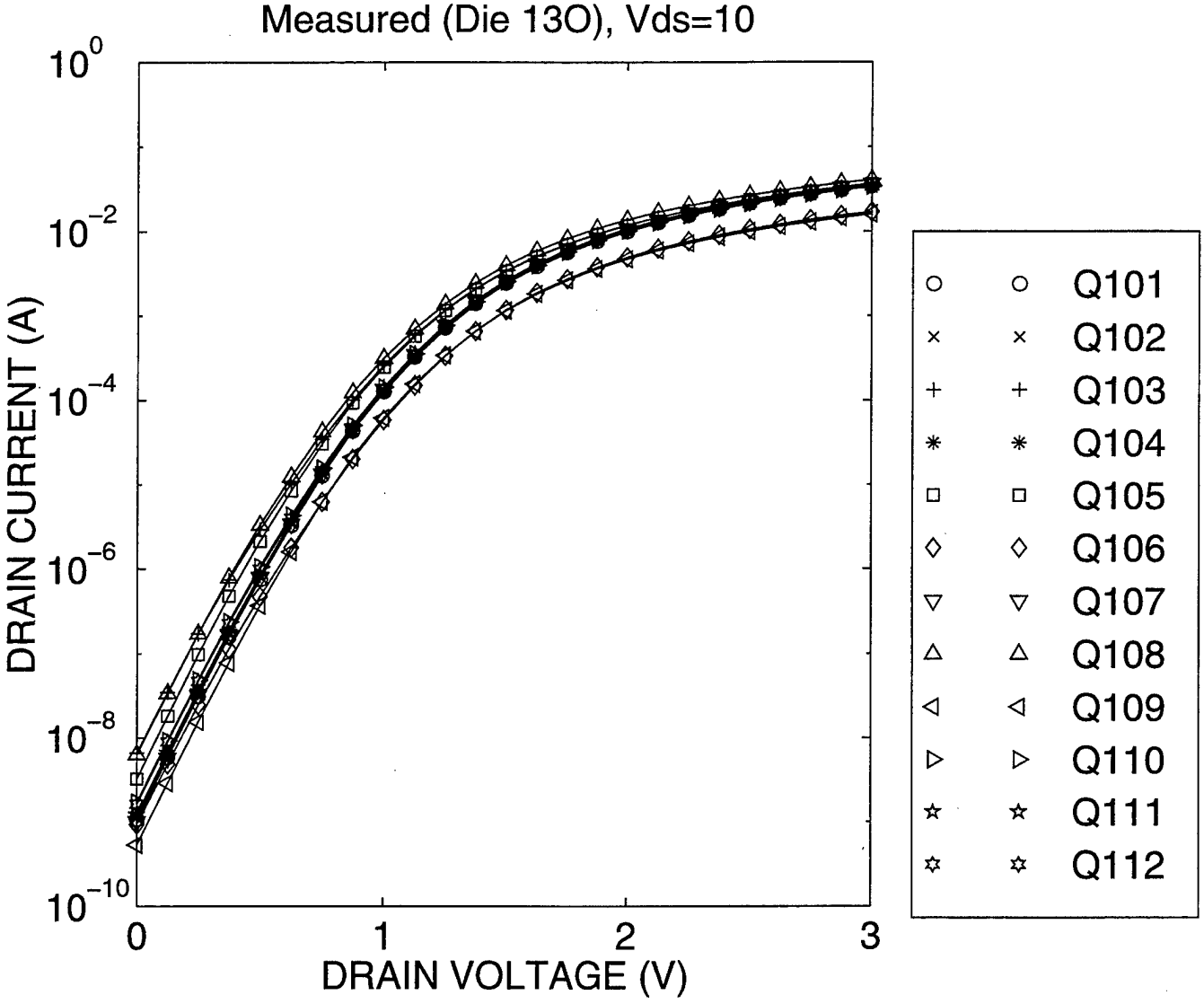

Measured (Die 6E), Vds=0.1
DRAIN CURRENT (A)
DRAIN VOLTAGE (V)
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
0
1
2
3
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

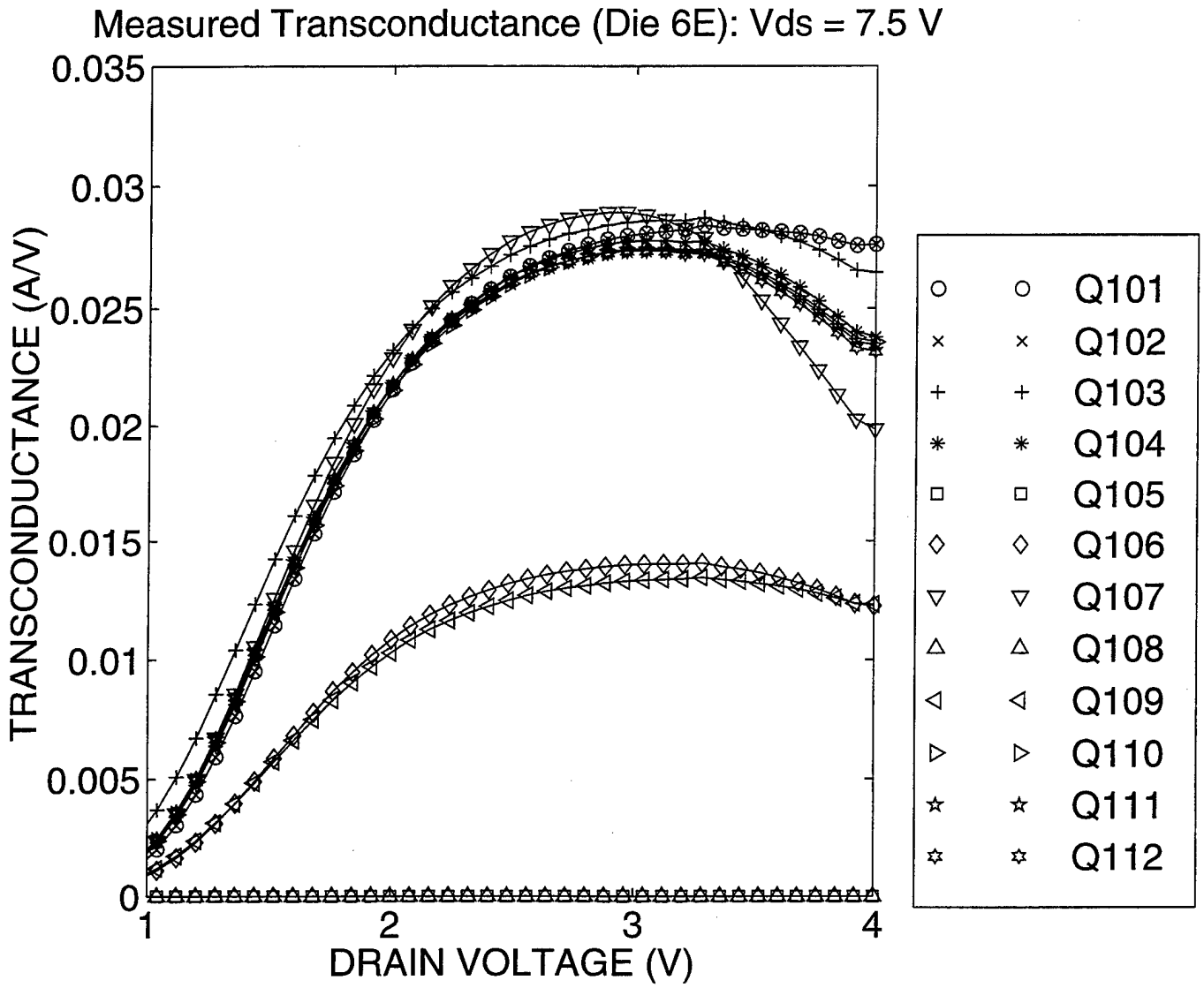

Measured (Die 6E), Vds=10
DRAIN CURRENT (A)
DRAIN VOLTAGE (V)
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
0
1
2
3
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

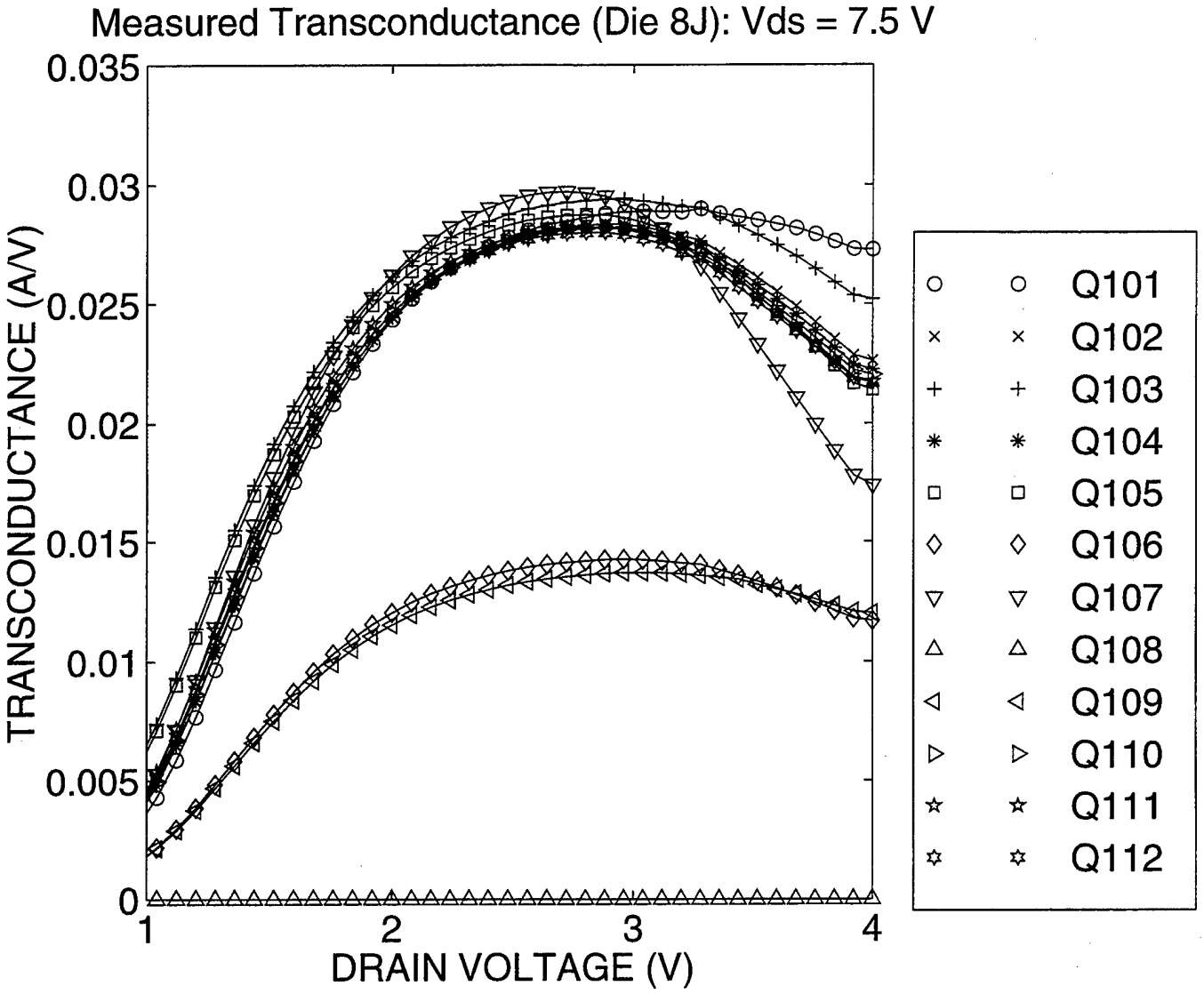

Measured (Die 8J), Vds=0.1
DRAIN CURRENT (A)
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
0
1
2
3
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

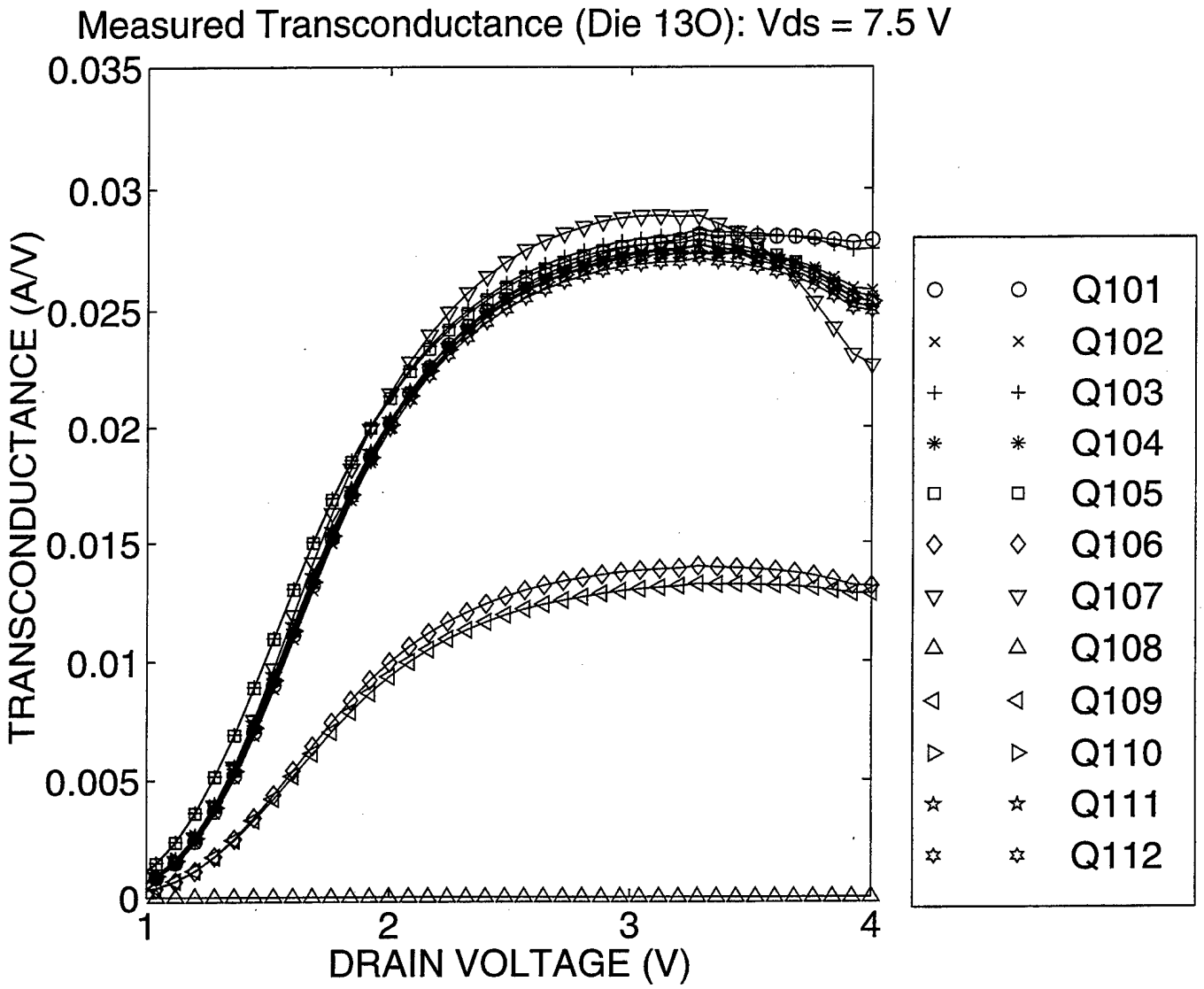

Measured (Die 8J), Vds=10
DRAIN CURRENT (A)
DRAIN VOLTAGE (V)
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
0
1
2
3
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

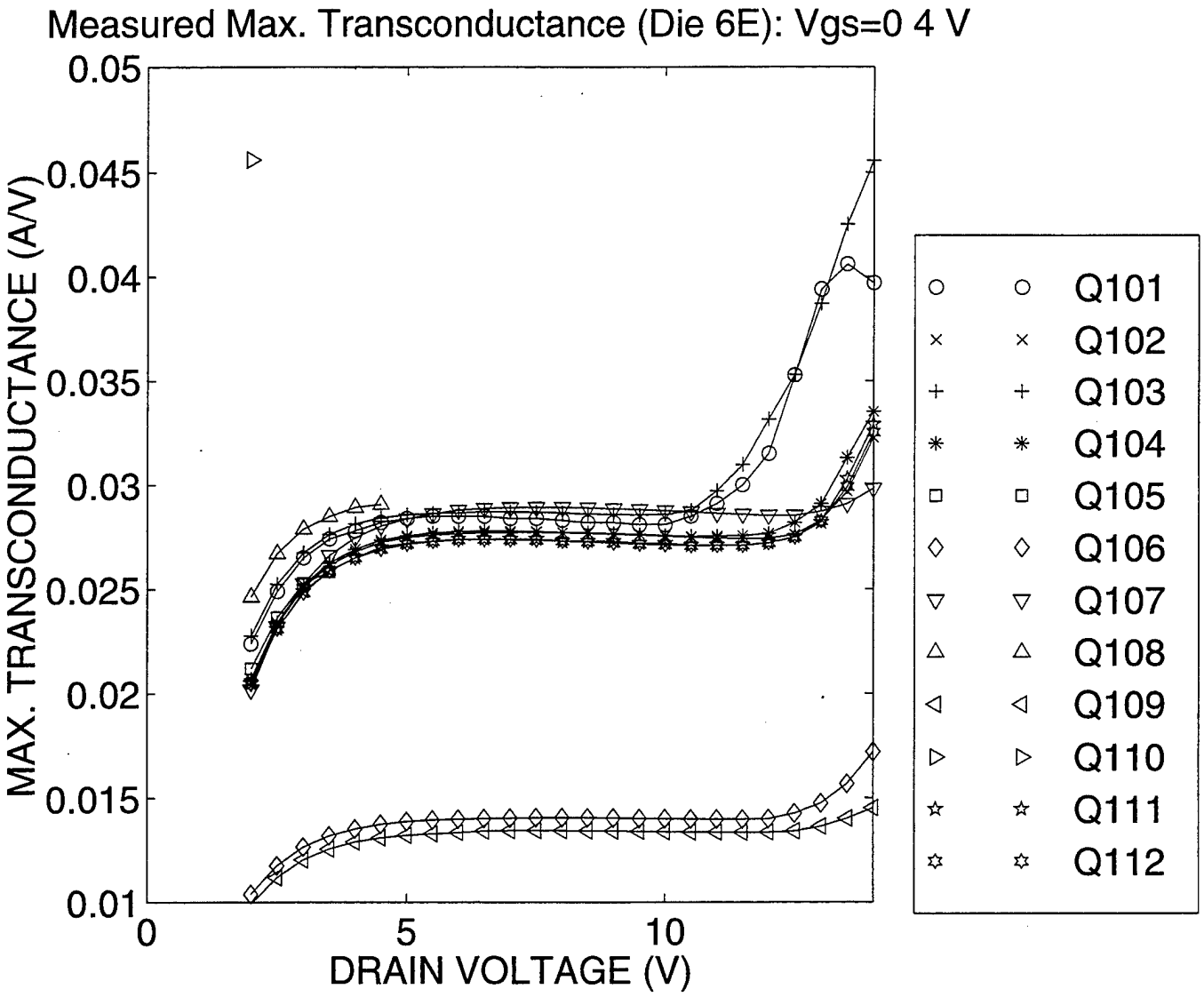

Measured (Die 13O), Vds=0.1
DRAIN CURRENT (A)
DRAIN VOLTAGE (V)
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
0
1
2
3
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

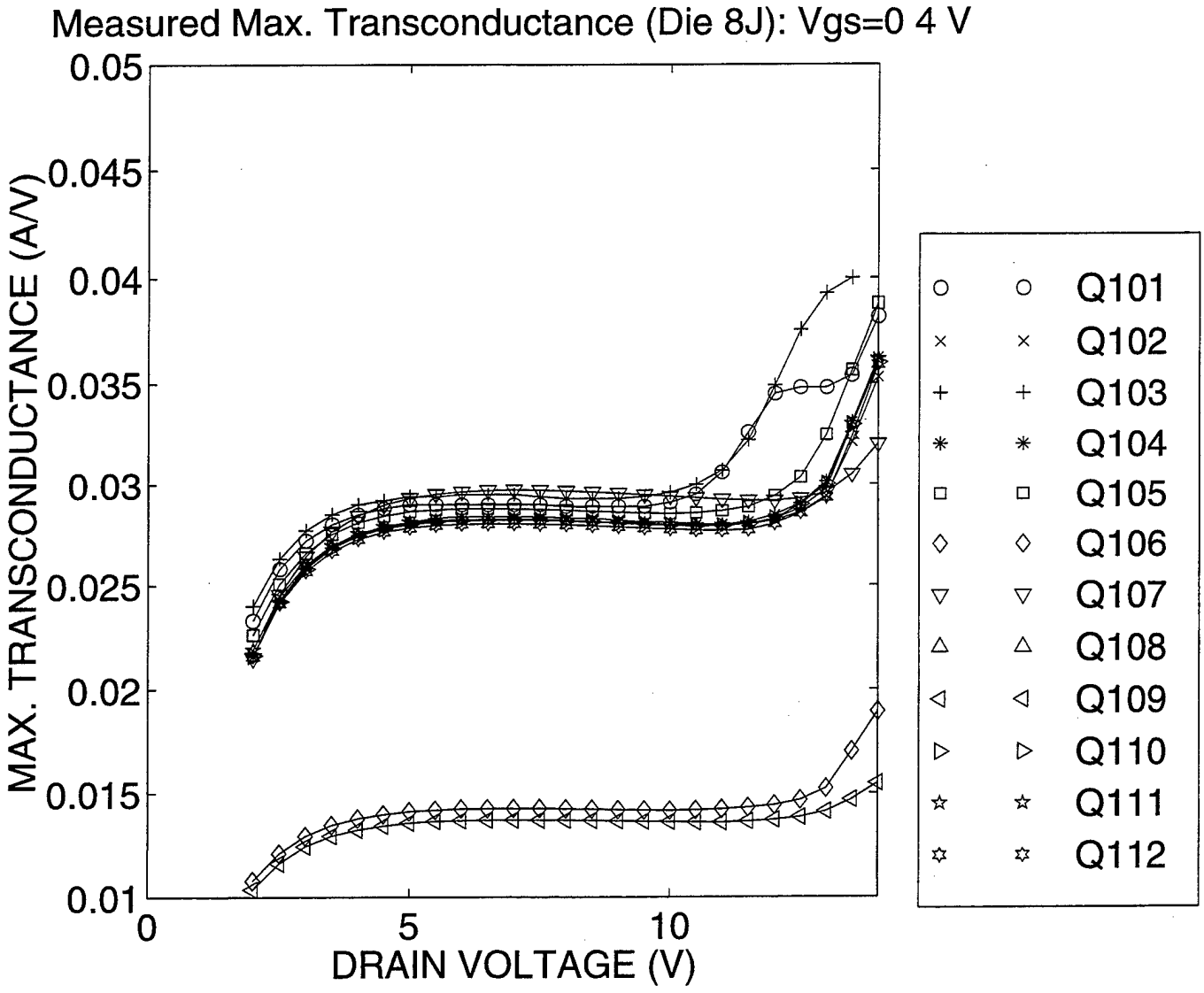

Measured (Die 13O), Vds=10
DRAIN CURRENT (A)
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
0
1
2
3
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

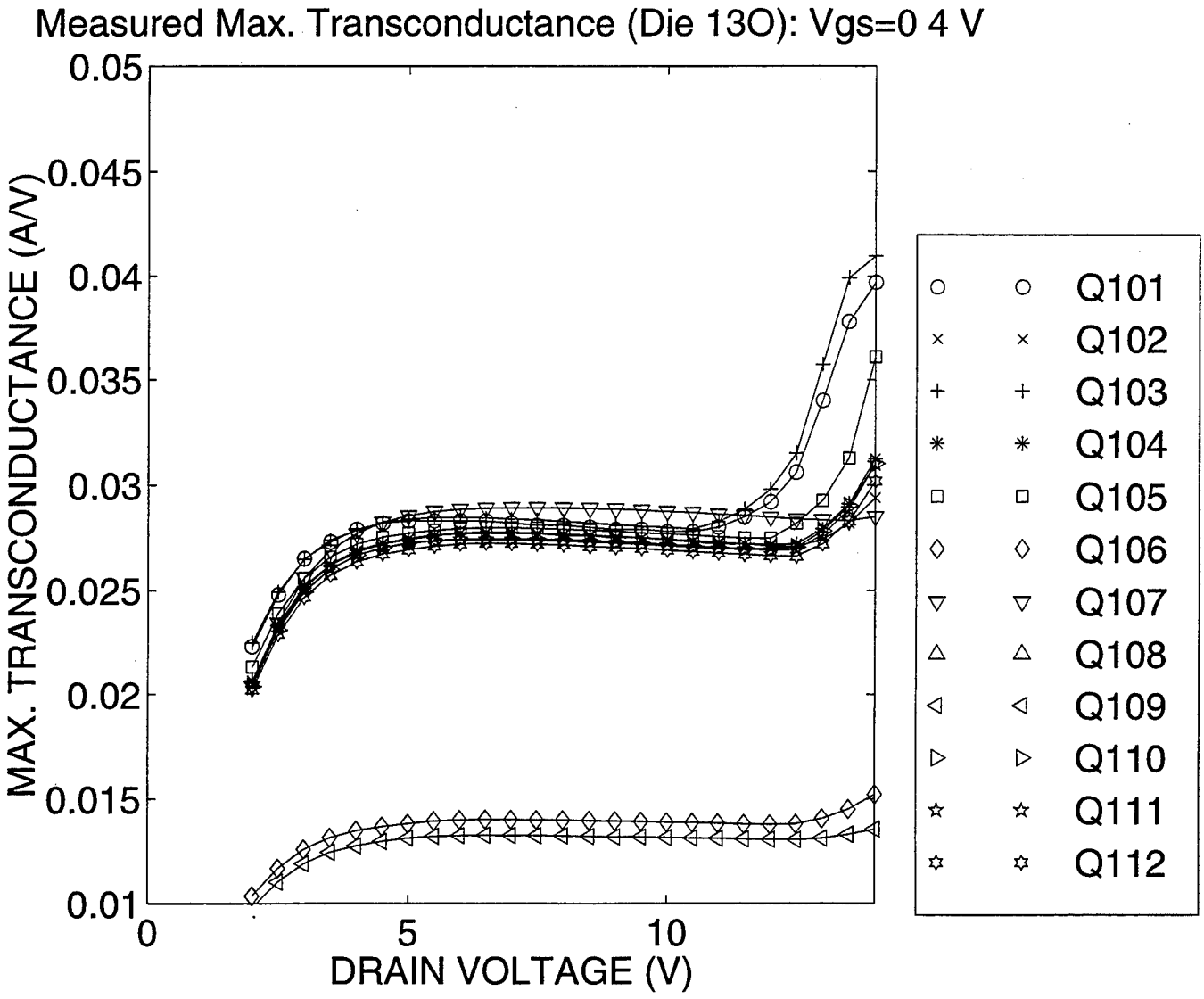

Measured Transconductance (Die 6E): Vds = 7.5 V
TRANSCONDUCTANCE (A/V)
0.035
0.03
0.025
0.02
0.015
0.01
0.005
0
1
2
3
4
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

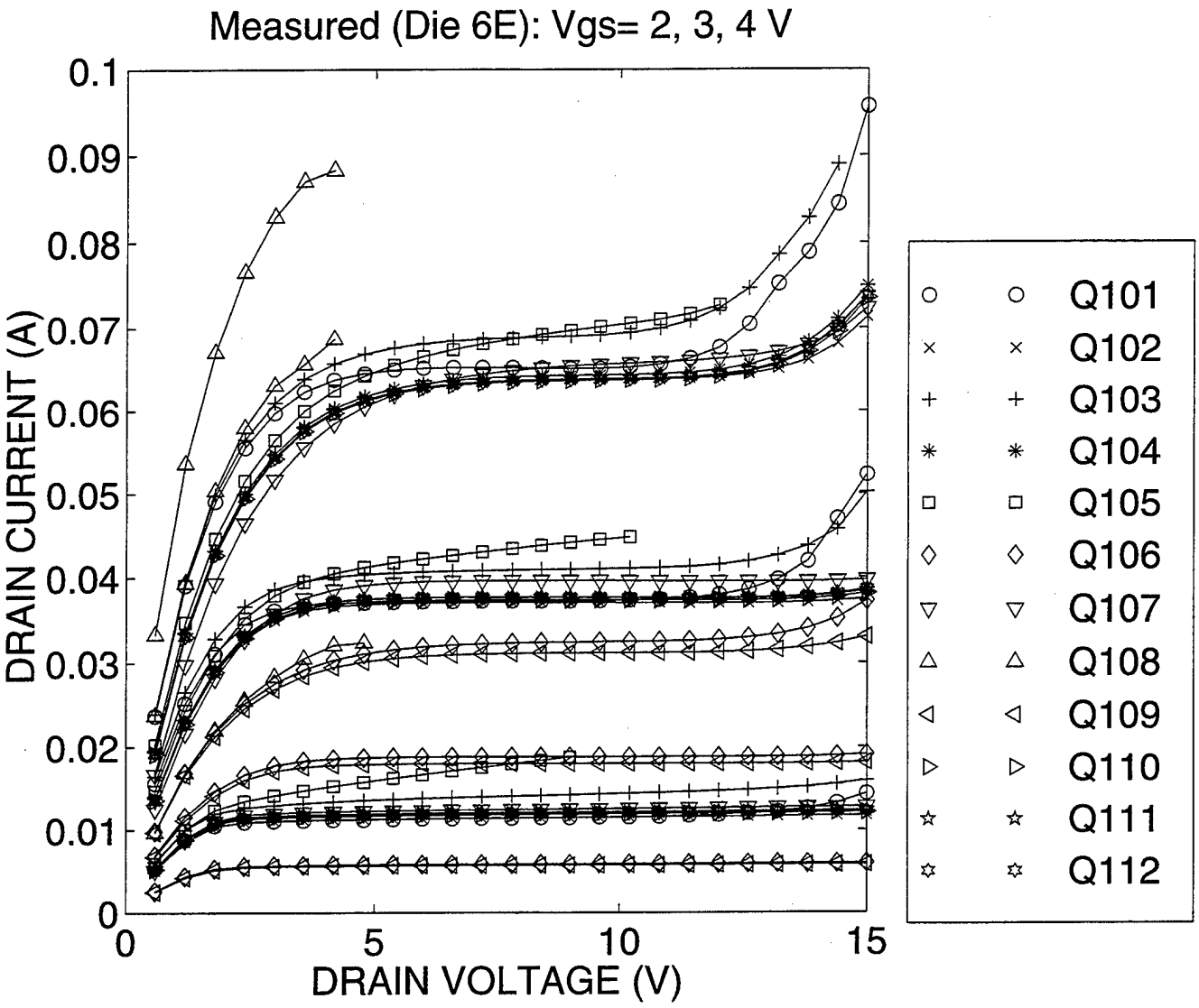

Measured Transconductance (Die 8J): Vds = 7.5 V
TRANSCONDUCTANCE (A/V)
0.035
0.03
0.025
0.02
0.015
0.01
0.005
0
1
2
3
4
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

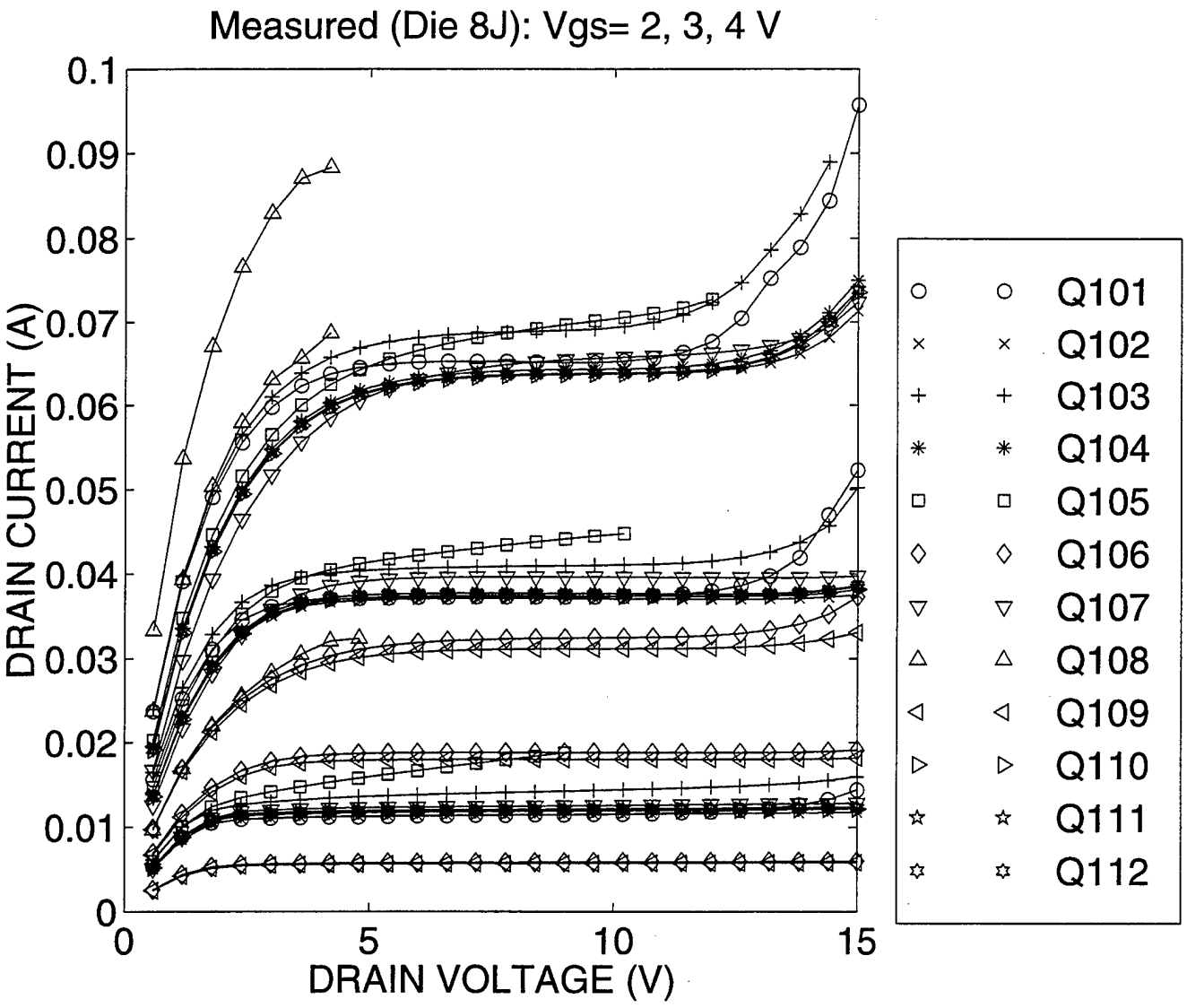

Measured Transconductance (Die 13O): Vds = 7.5 V
TRANSCONDUCTANCE (A/V)
0.035
0.03
0.025
0.02
0.015
0.01
0.005
0
1
2
3
4
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

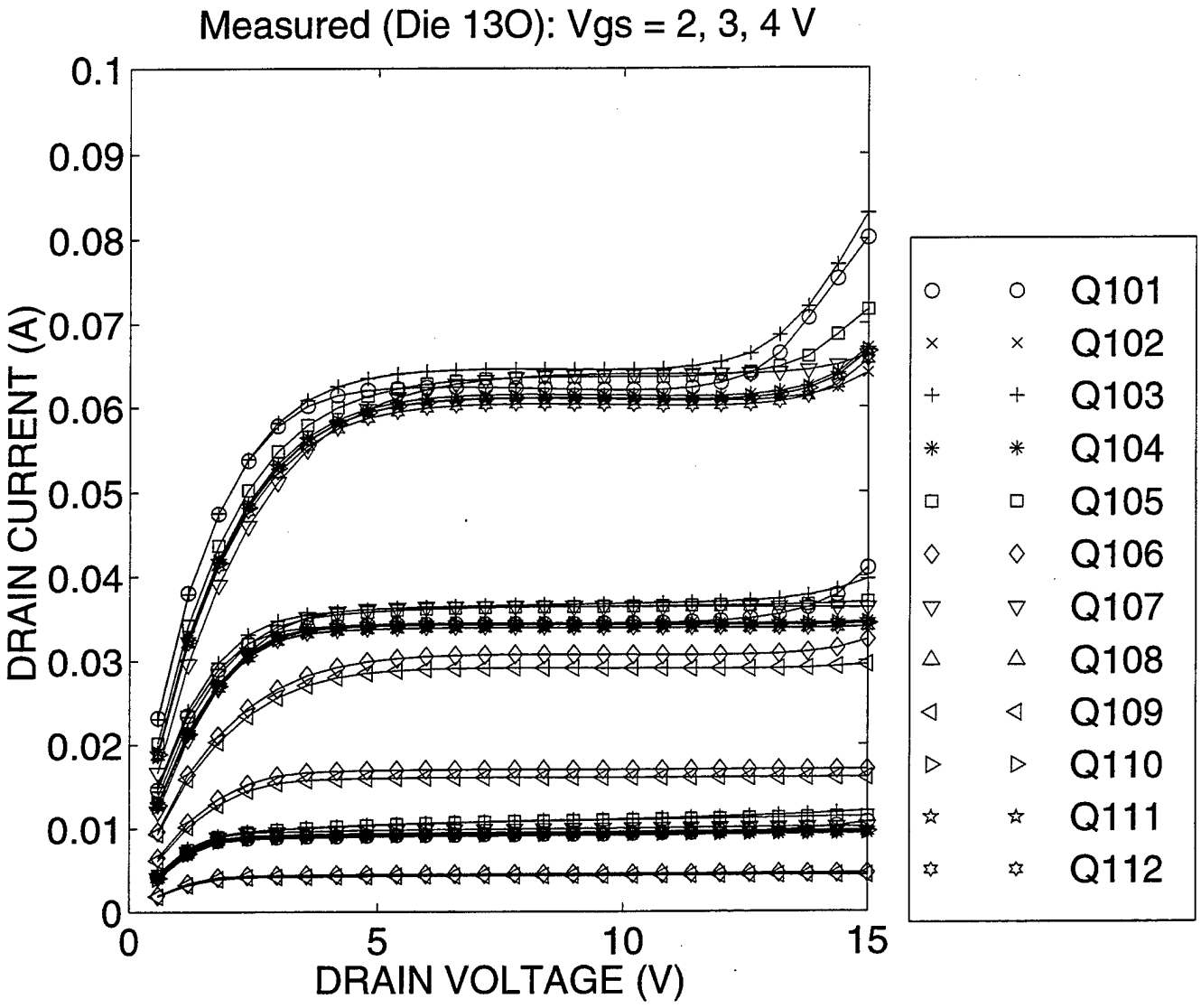

Measured Max. Transconductance (Die 6E): Vgs=0 4 V
MAX. TRANSCONDUCTANCE (A/V)
0.05
0.045
0.04
0.035
0.03
0.025
0.02
0.015
0.01
0
5
10
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112


Measured Max. Transconductance (Die 8J): Vgs=0 4 V
MAX. TRANSCONDUCTANCE (A/V)
0.05
0.045
0.04
0.035
0.03
0.025
0.02
0.015
0.01
0
5
10
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

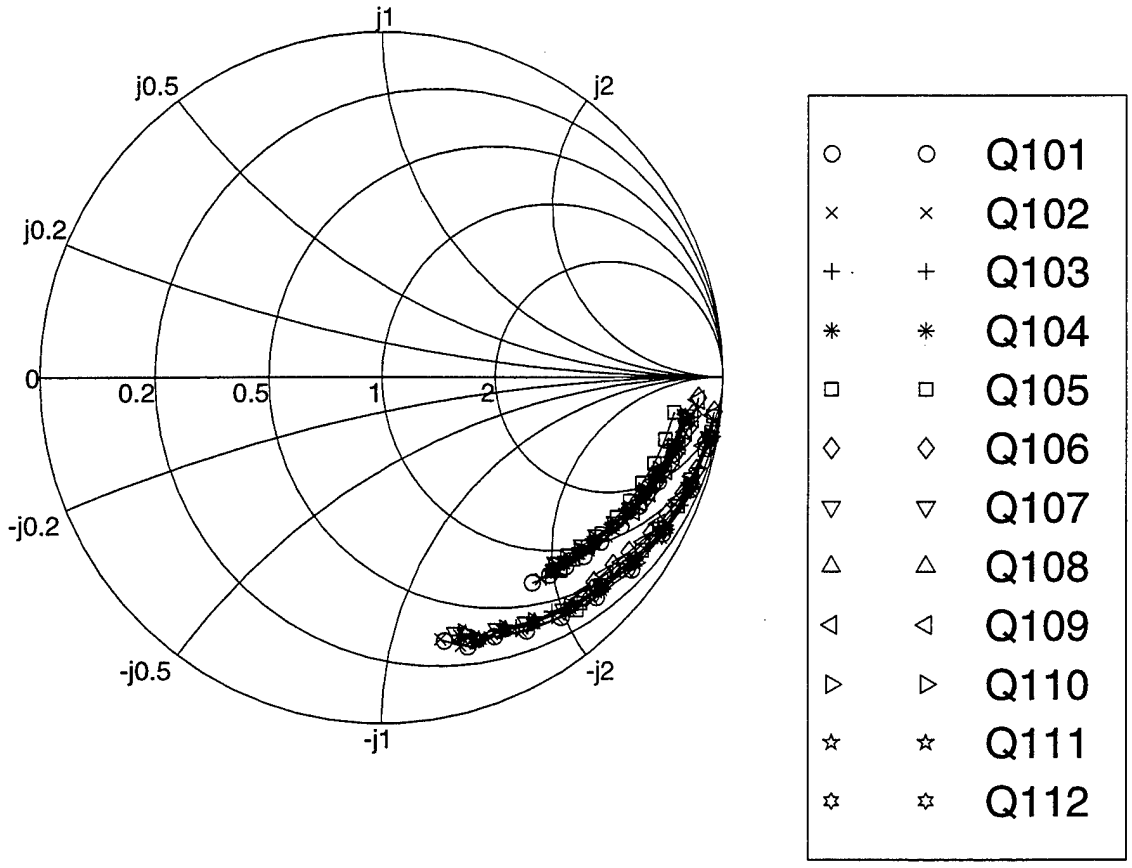

Measured Max. Transconductance (Die 13O): Vgs=0 4 V
MAX. TRANSCONDUCTANCE (A/V)
0.05
0.045
0.04
0.035
0.03
0.025
0.02
0.015
0.01
0
5
10
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112


Measured (Die 6E): Vgs= 2, 3, 4 V
DRAIN CURRENT (A)
0.1
0.09
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
0
5
10
15
DRAIN VOLTAGE (V)
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

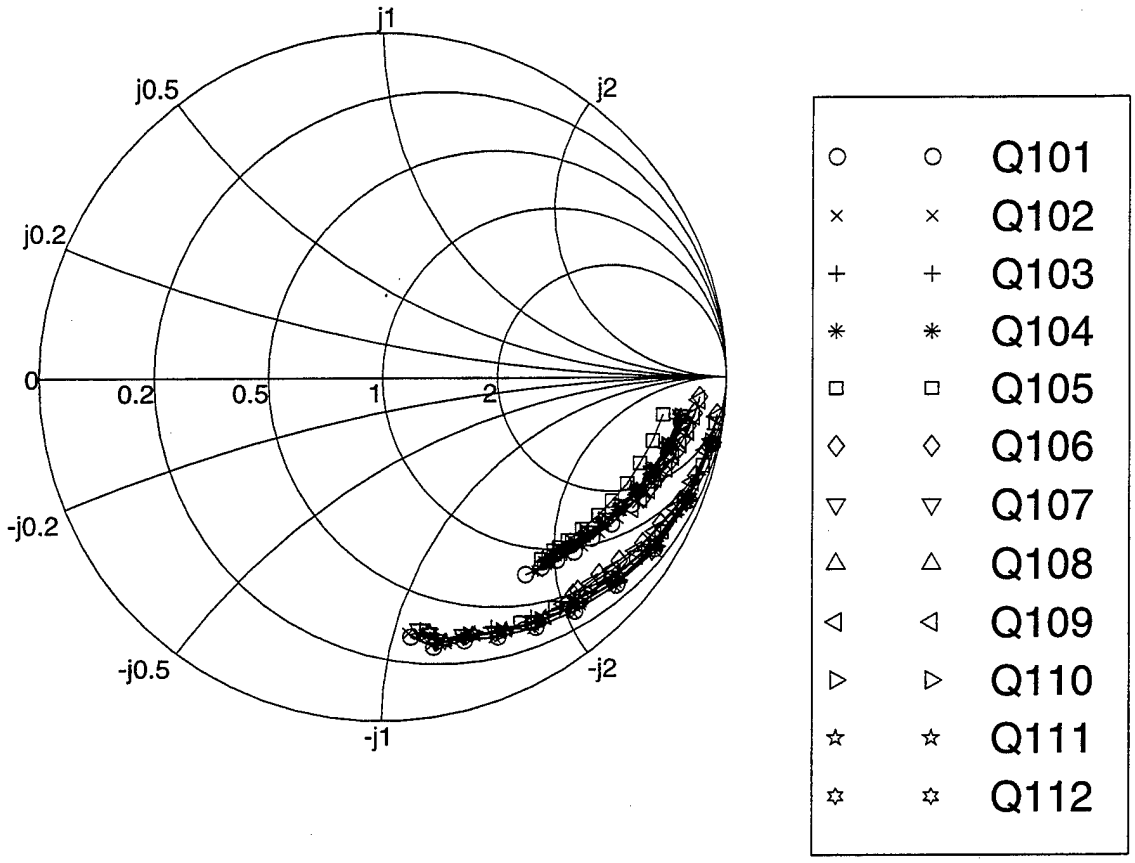

Measured (Die 8J): Vgs= 2, 3, 4 V
DRAIN CURRENT (A)
DRAIN VOLTAGE (V)
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
0
5
10
15
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112


Measured (Die 13O): Vgs = 2, 3, 4 V
DRAIN CURRENT (A)
DRAIN VOLTAGE (V)
0.1
0.09
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
0
5
10
15
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

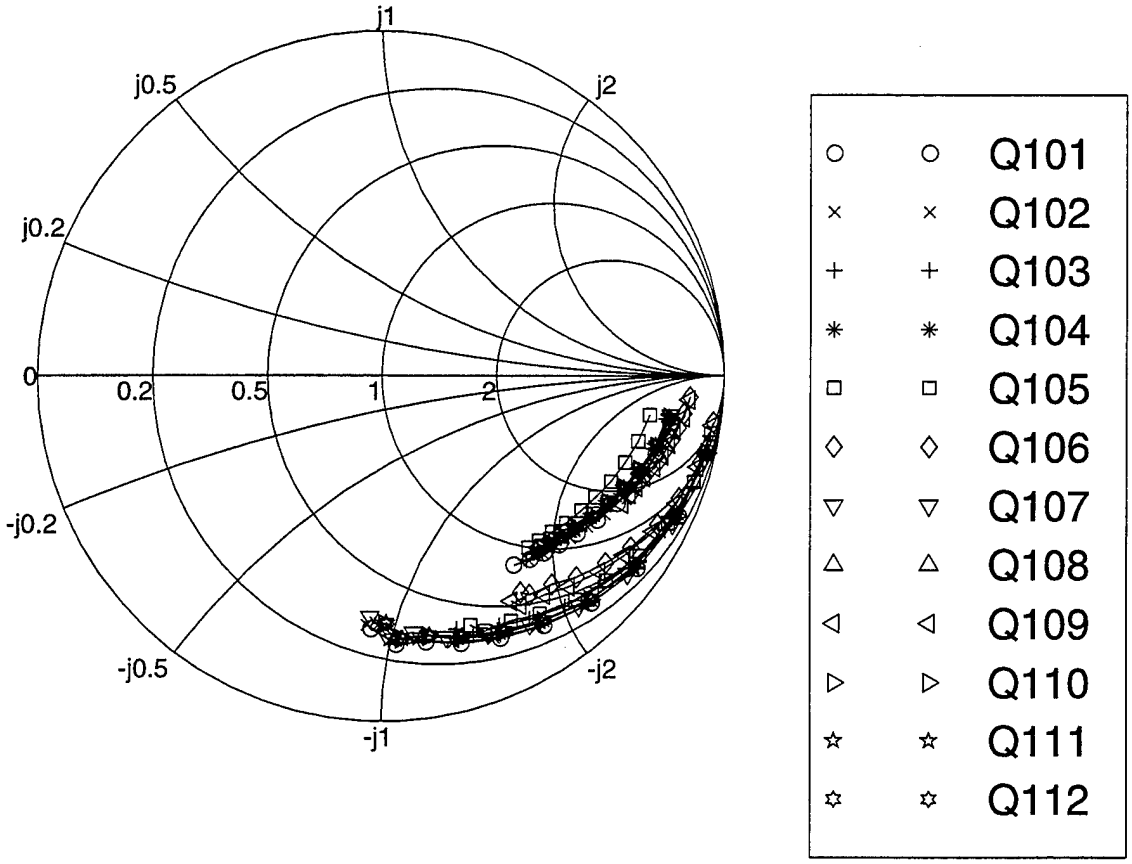
Measured S11 and S22 (Die 6E): Id = 5 mA



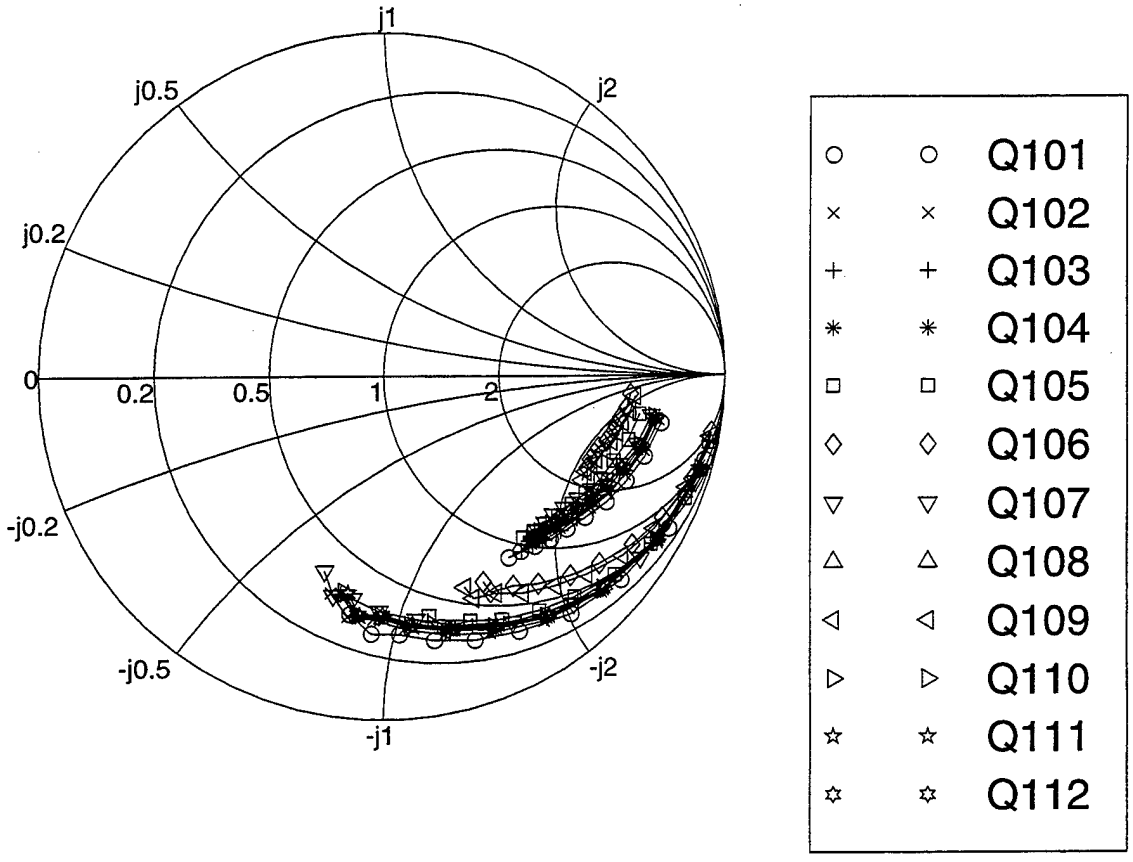
Measured S11 and S22 (Die 6E): Id = 10 mA



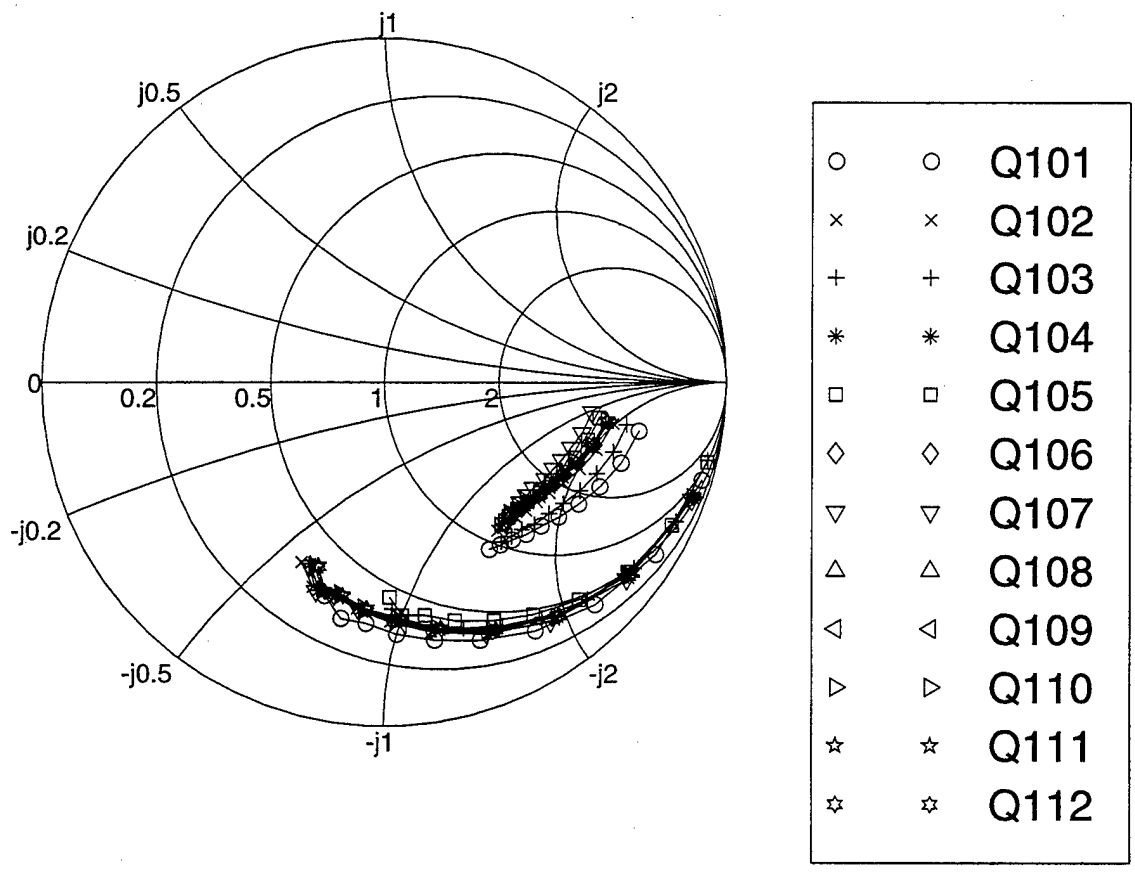
Measured S11 and S22 (Die 6E): Id = 25 mA



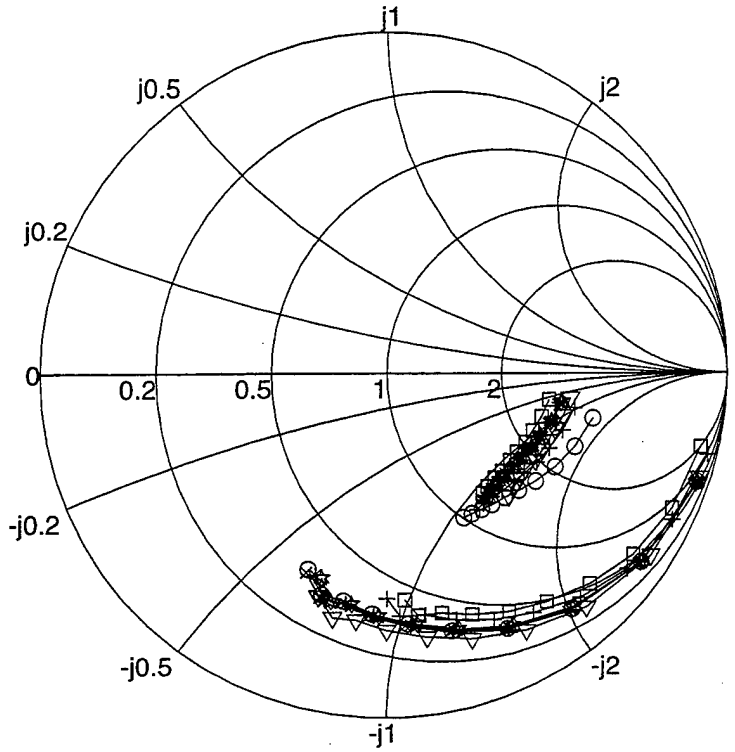
Measured S11 and S22 (Die 6E): Id = 50 mA



Measured S11 and S22 (Die 6E): Id = 75 mA

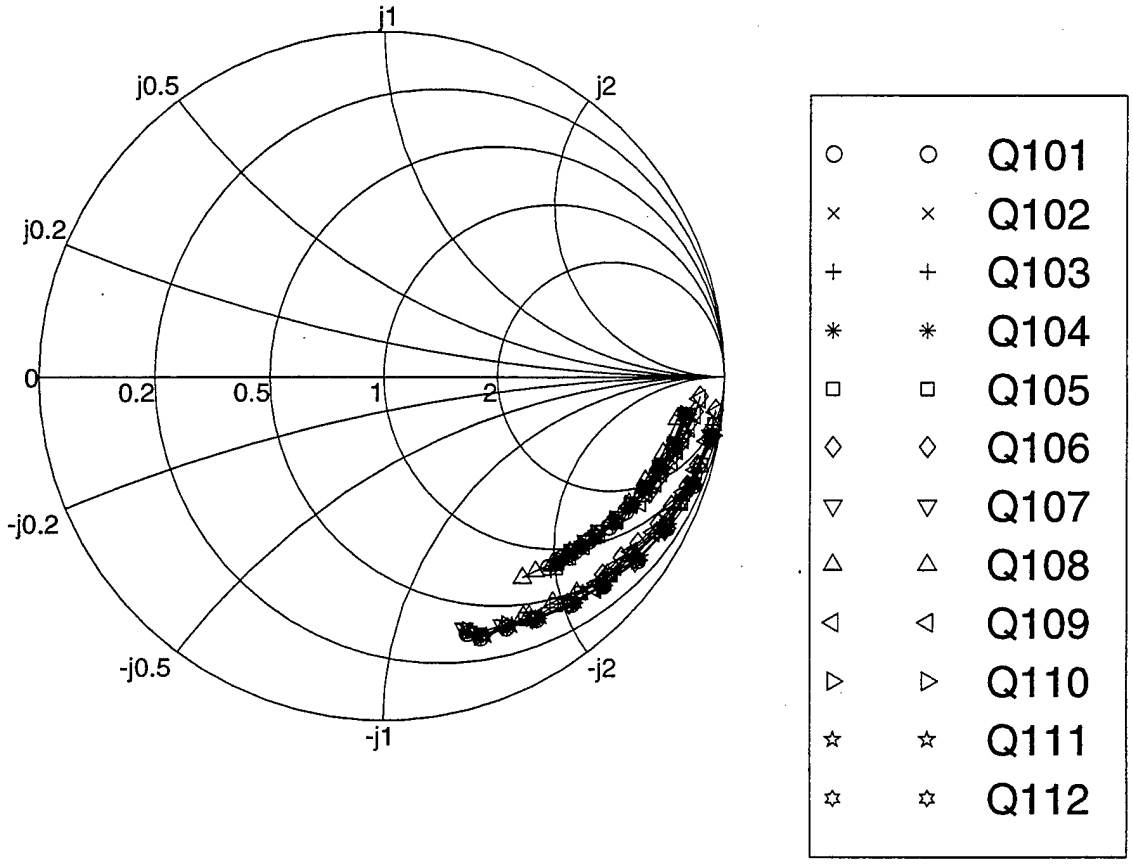


Measured S11 and S22 (Die 6E): Id = 100 mA

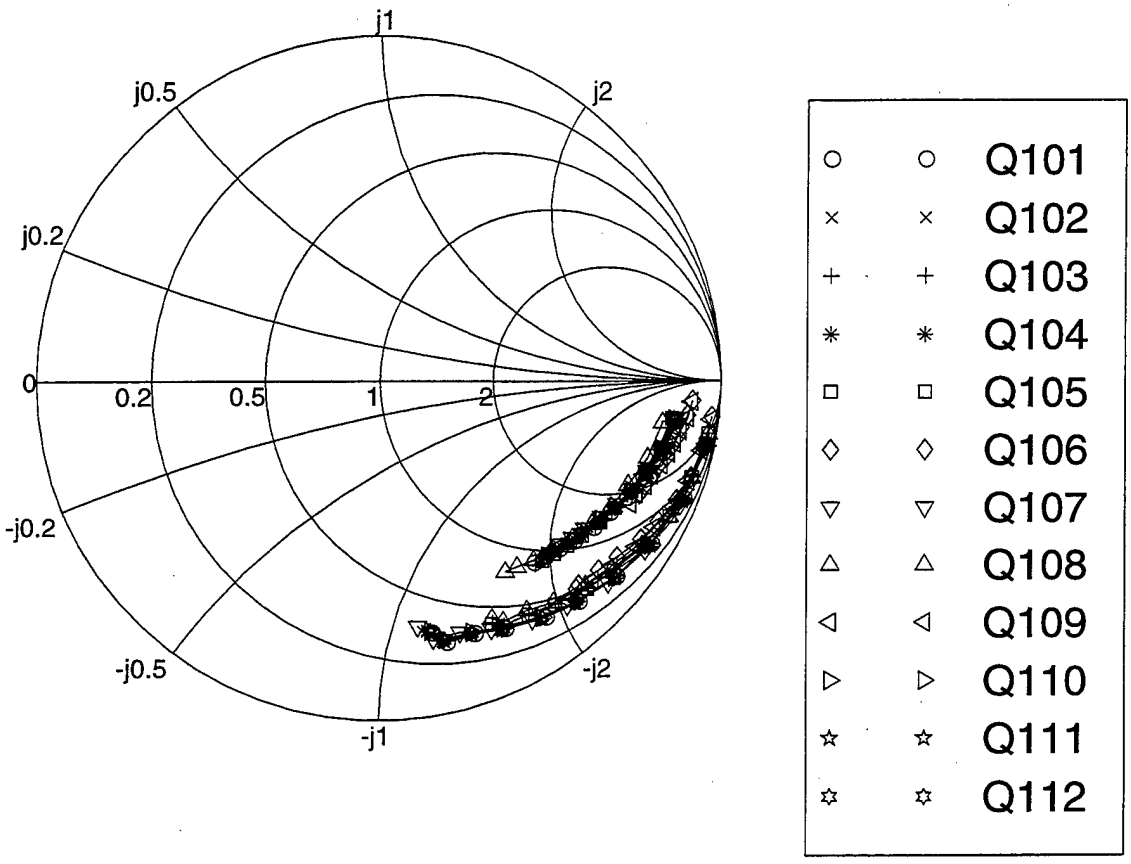


○	○	Q101
×	×	Q102
+	+	Q103
✳	✳	Q104
□	□	Q105
◇	◇	Q106
▽	▽	Q107
△	△	Q108
◁	◁	Q109
▷	▷	Q110
☆	☆	Q111
✡	✡	Q112

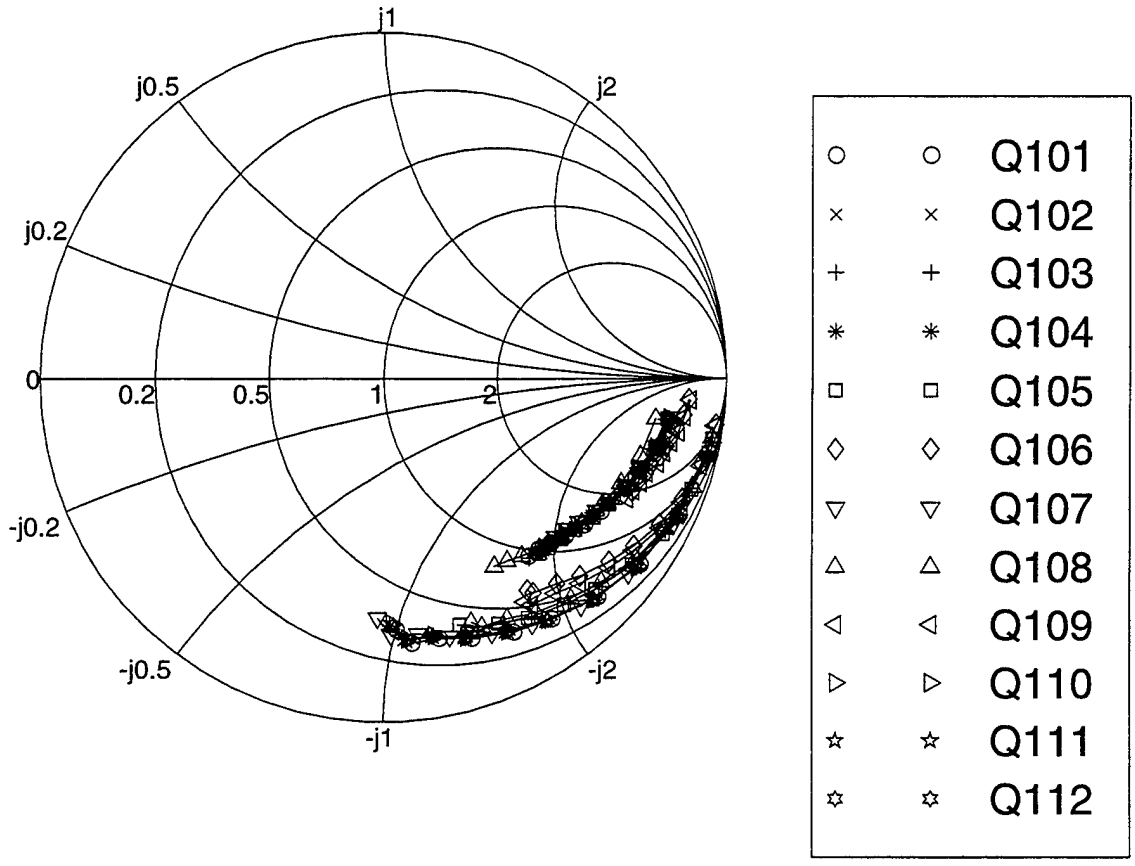
Measured S11 and S22 (Die 8J): Id = 5 mA



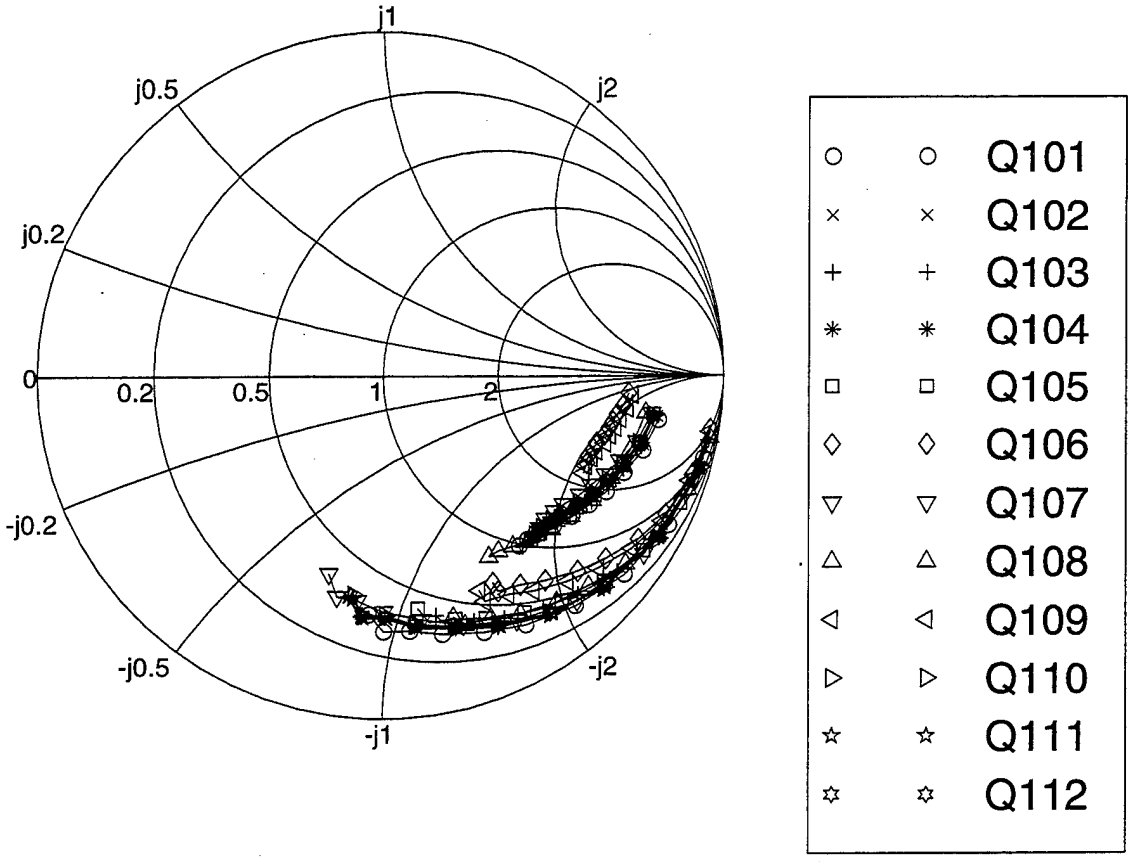
Measured S11 and S22 (Die 8J): Id = 10 mA



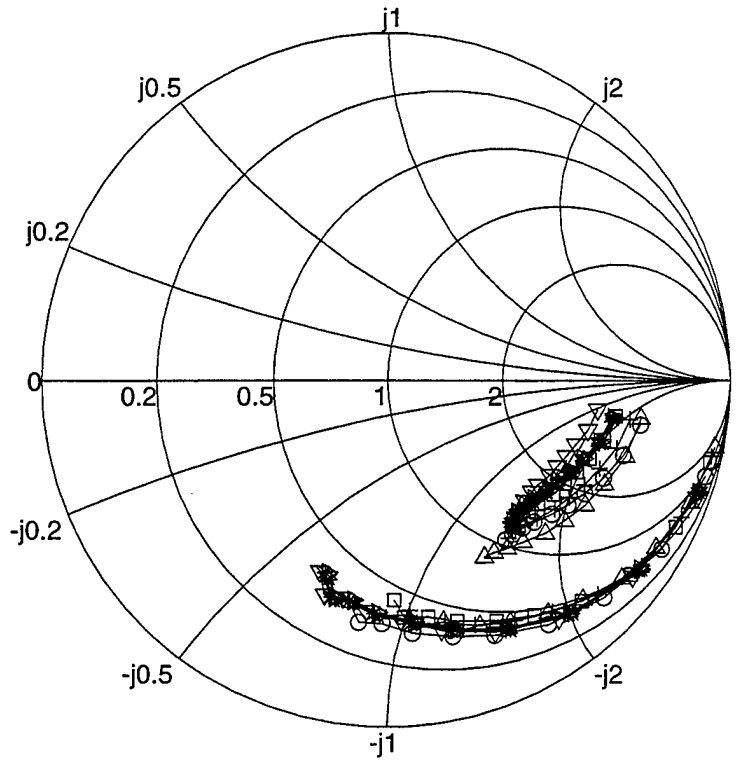
Measured S11 and S22 (Die 8J): Id = 25 mA



Measured S11 and S22 (Die 8J): Id = 50 mA

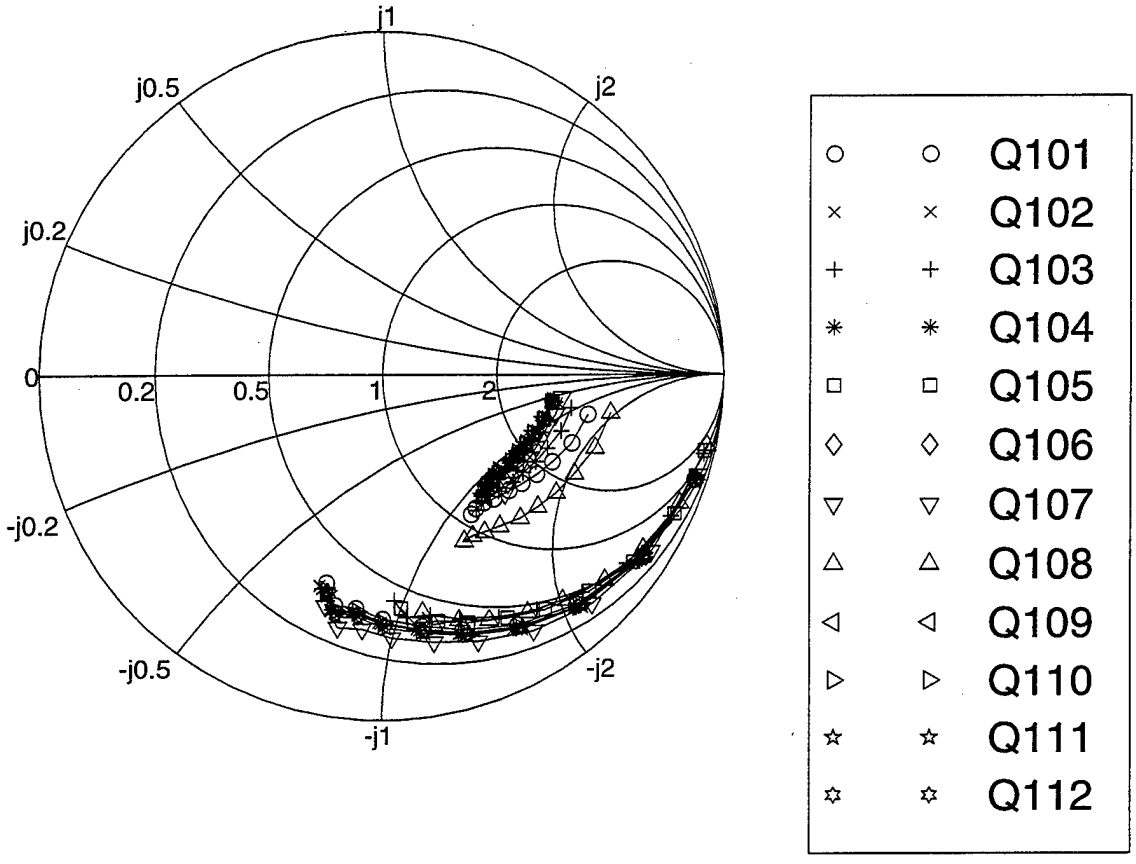


Measured S11 and S22 (Die 8J): Id = 75 mA

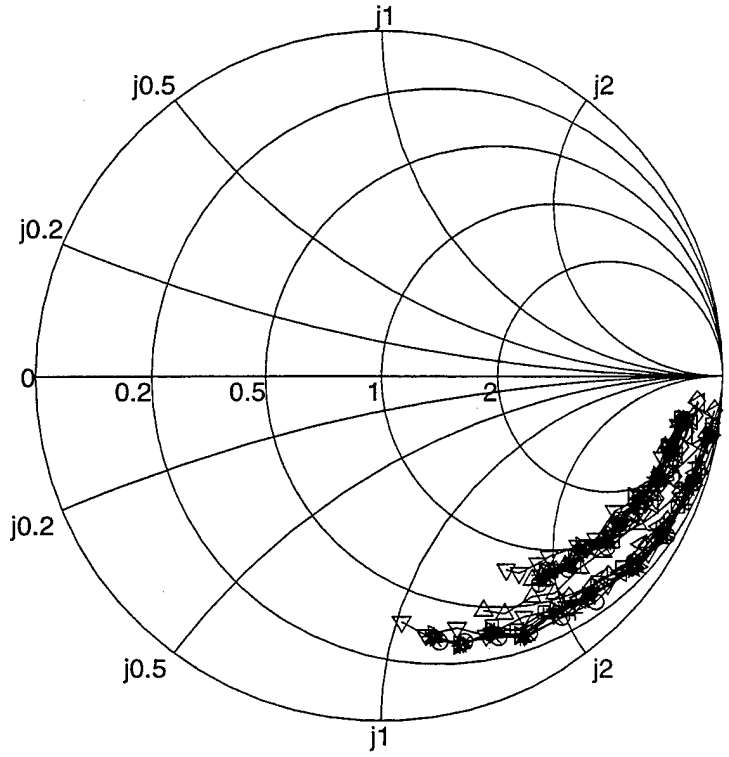


○	○	Q101
×	×	Q102
+	+	Q103
✳	✳	Q104
□	□	Q105
◇	◇	Q106
▽	▽	Q107
△	△	Q108
◁	◁	Q109
▷	▷	Q110
☆	☆	Q111
✡	✡	Q112

Measured S11 and S22 (Die 8J): Id = 100 mA

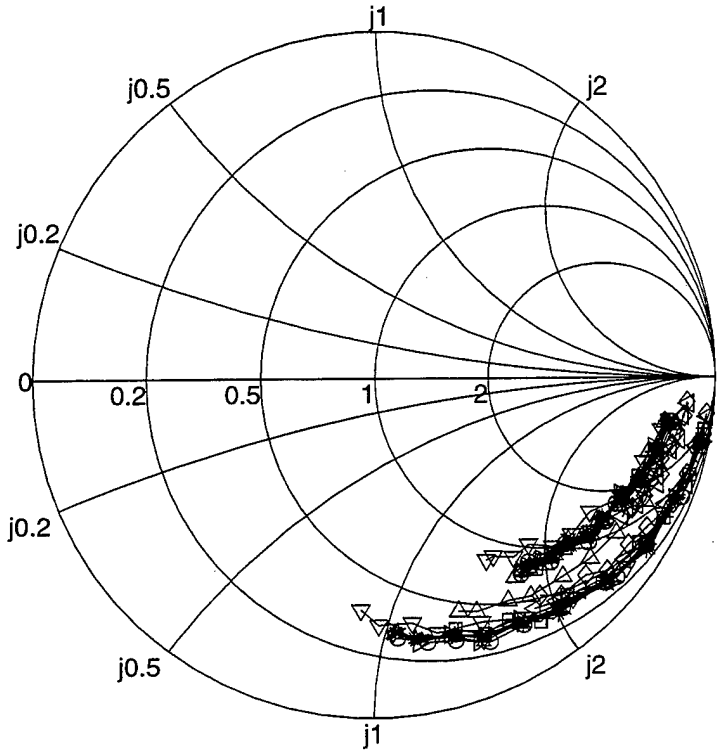


Measured S11 and S22 (Die 13O): Id = 5 mA



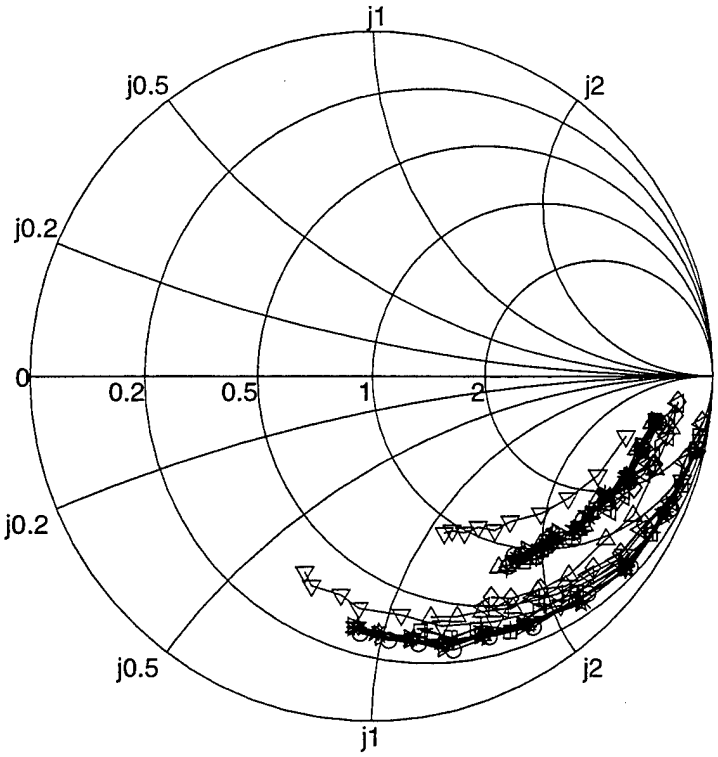
○	○	Q101
×	×	Q102
+	+	Q103
✳	✳	Q104
□	□	Q105
◇	◇	Q106
▽	▽	Q107
△	△	Q108
◁	◁	Q109
▷	▷	Q110
☆	☆	Q111
✡	✡	Q112

Measured S11 and S22 (Die 13O): Id = 10 mA



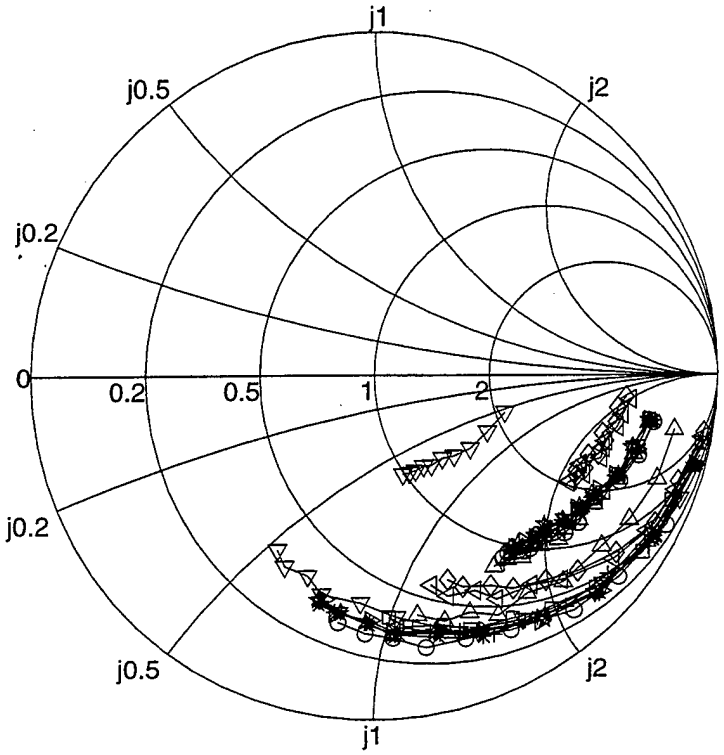
○	○	Q101
×	×	Q102
+	+	Q103
✳	✳	Q104
□	□	Q105
◇	◇	Q106
▽	▽	Q107
△	△	Q108
◁	◁	Q109
▷	▷	Q110
☆	☆	Q111
✡	✡	Q112

Measured S11 and S22 (Die 13O): Id = 25 mA



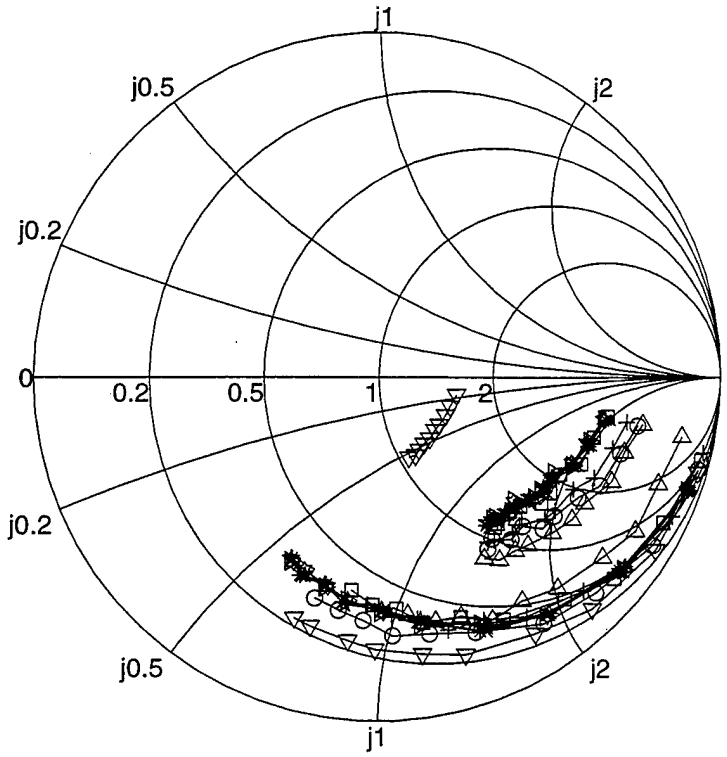
○	○	Q101
×	×	Q102
+	+	Q103
✳	✳	Q104
□	□	Q105
◇	◇	Q106
▽	▽	Q107
△	△	Q108
◁	◁	Q109
▷	▷	Q110
☆	☆	Q111
✡	✡	Q112

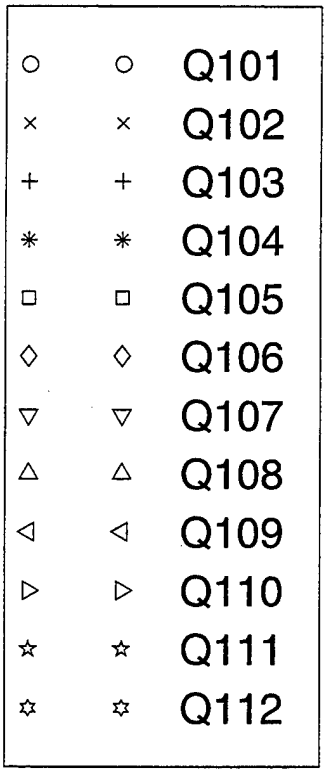
Measured S11 and S22 (Die 13O): Id = 50 mA



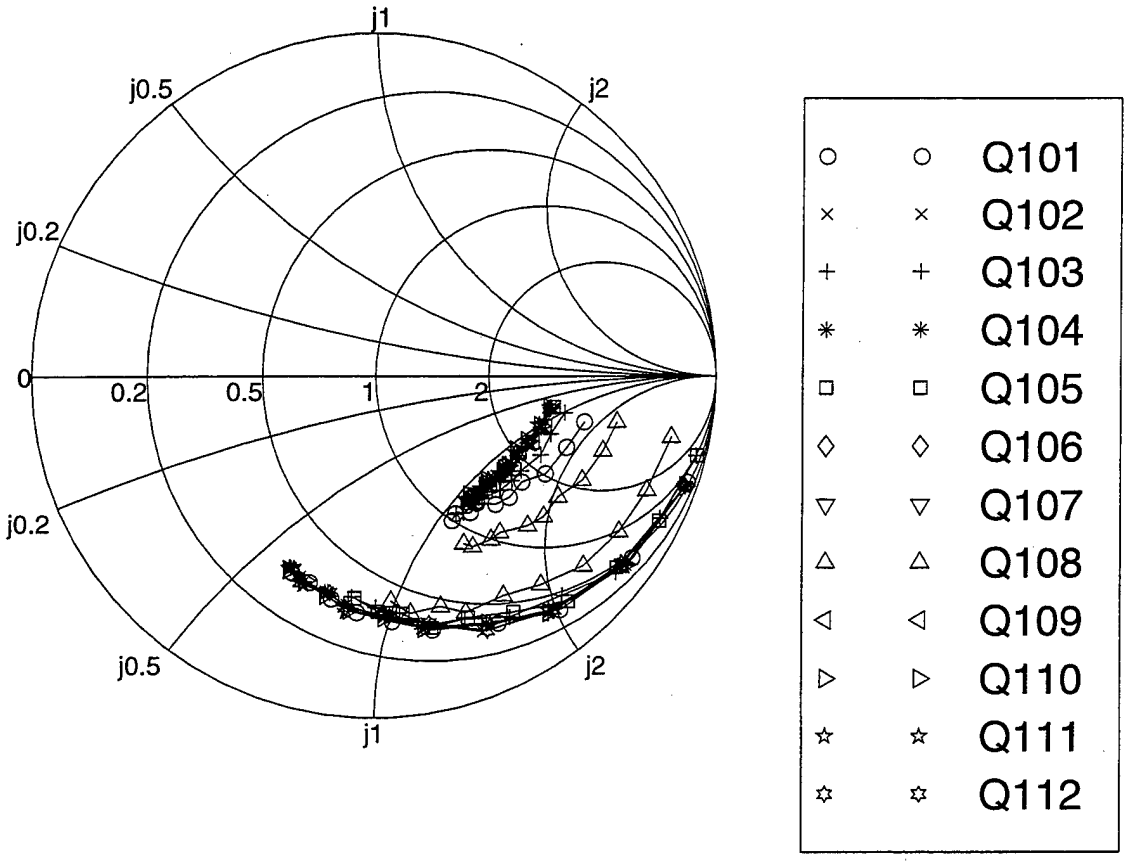
○	○	Q101
×	×	Q102
+	+	Q103
✳	✳	Q104
□	□	Q105
◇	◇	Q106
▽	▽	Q107
△	△	Q108
◁	◁	Q109
▷	▷	Q110
☆	☆	Q111
✡	✡	Q112

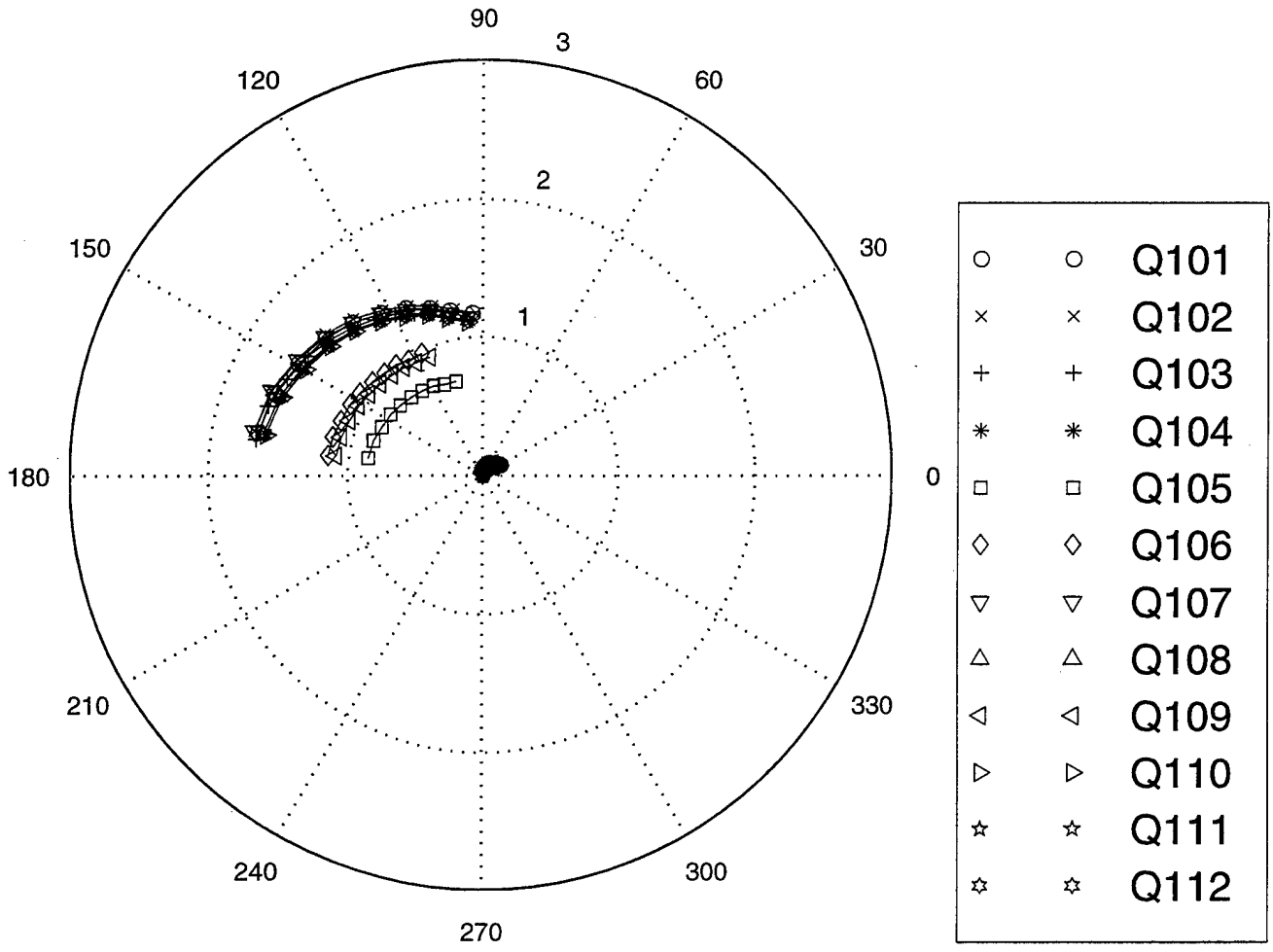
Measured S11 and S22 (Die 13O): Id = 75 mA

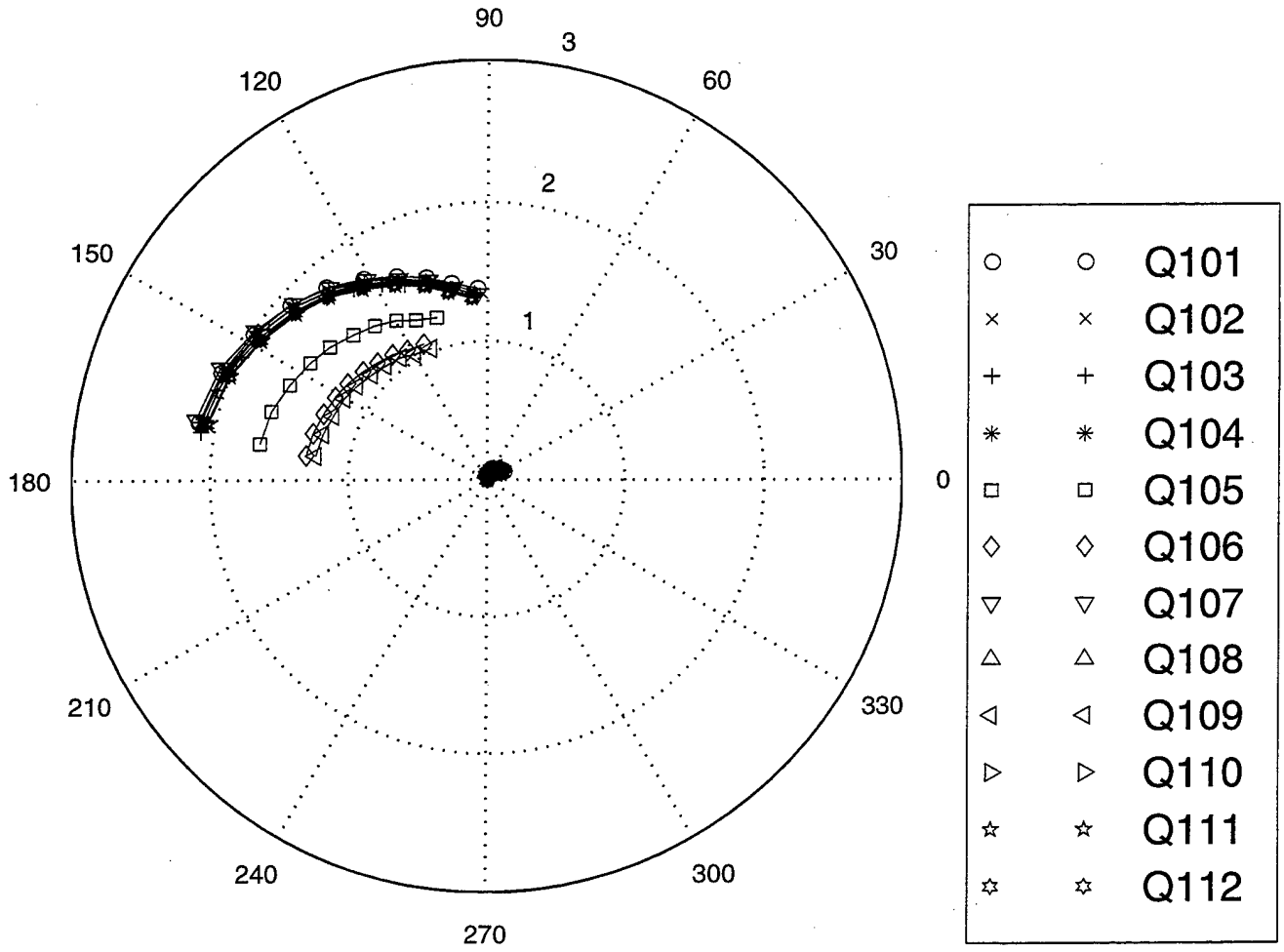


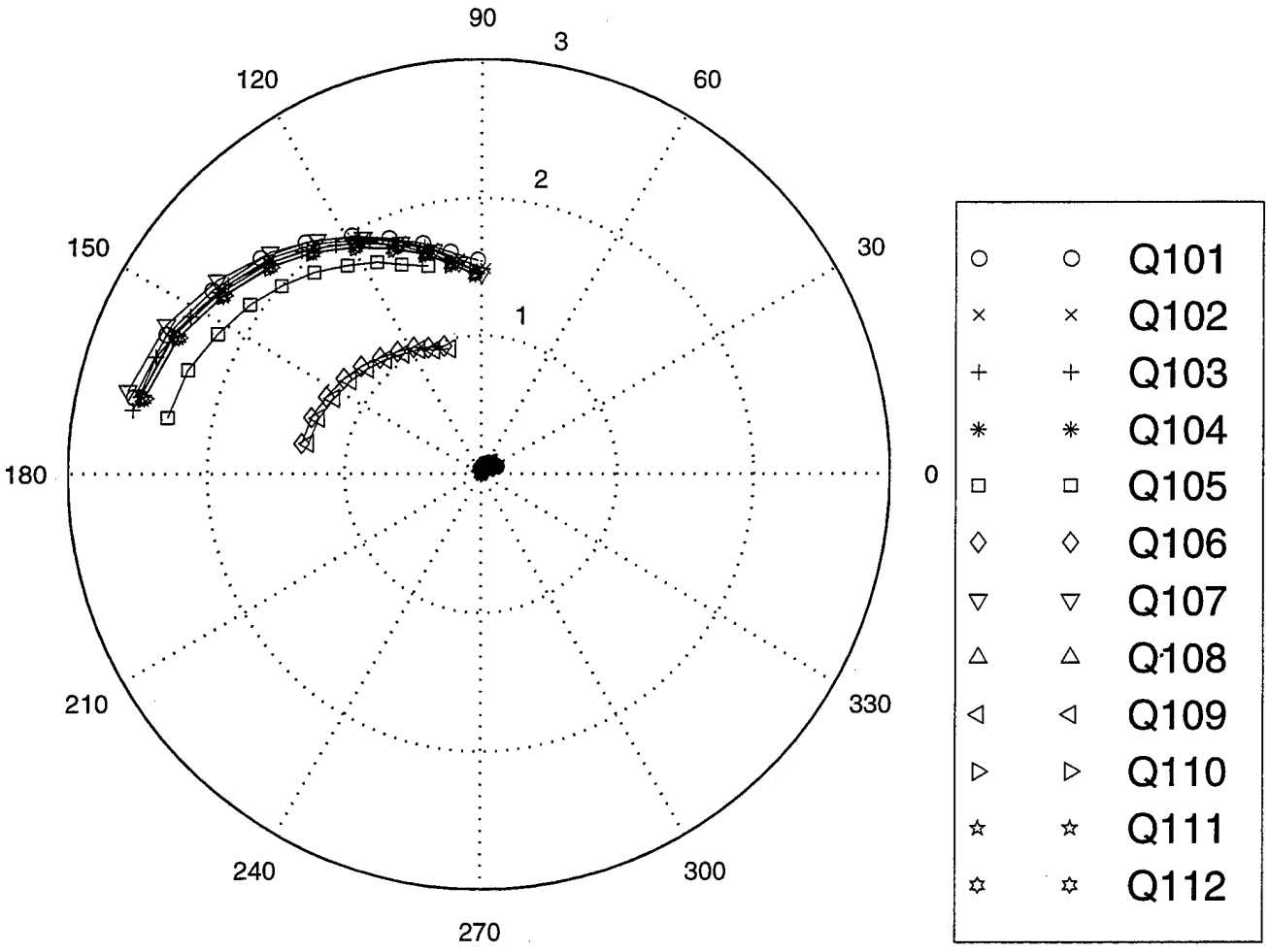


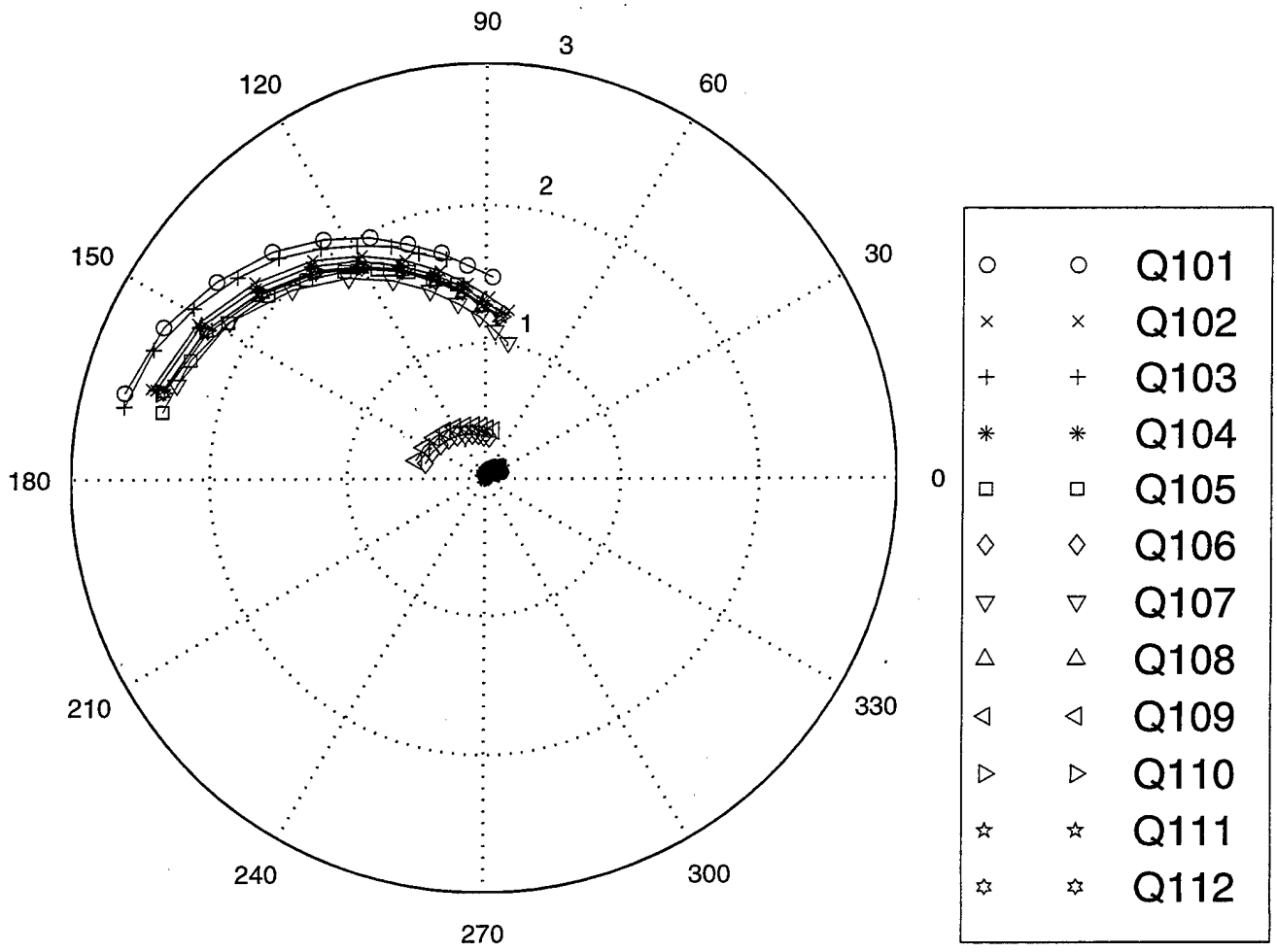
Measured S11 and S22 (Die 13O): Id = 100 mA



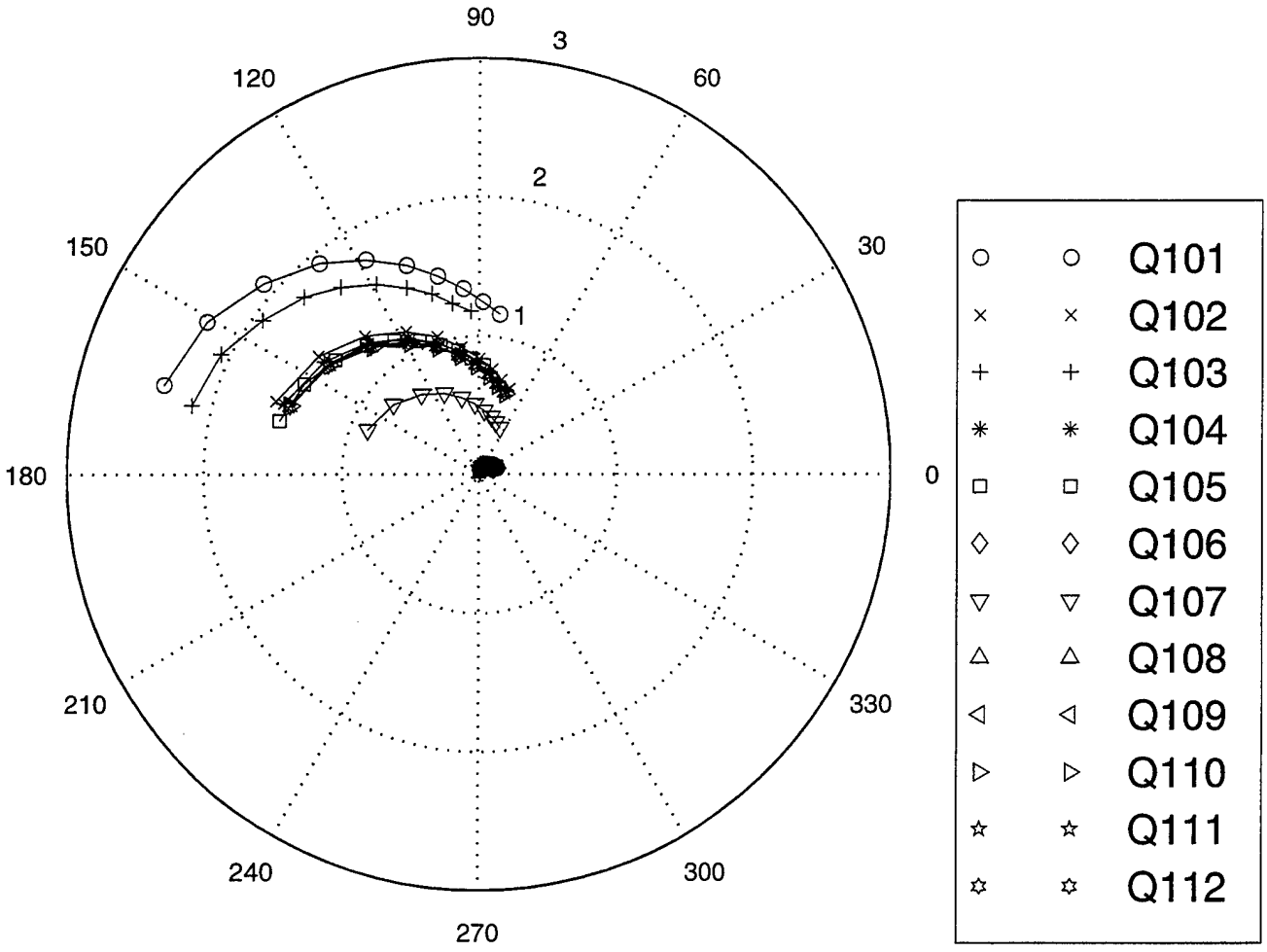

Measured S12 and S21 (Die 6E): Id = 5 mA
90
3
120
60
2
150
30
1
180
0
210
330
240
300
270
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112


Measured S12 and S21 (Die 6E): Id = 10 mA
90
3
120
60
2
150
30
1
180
0
210
330
240
300
270
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

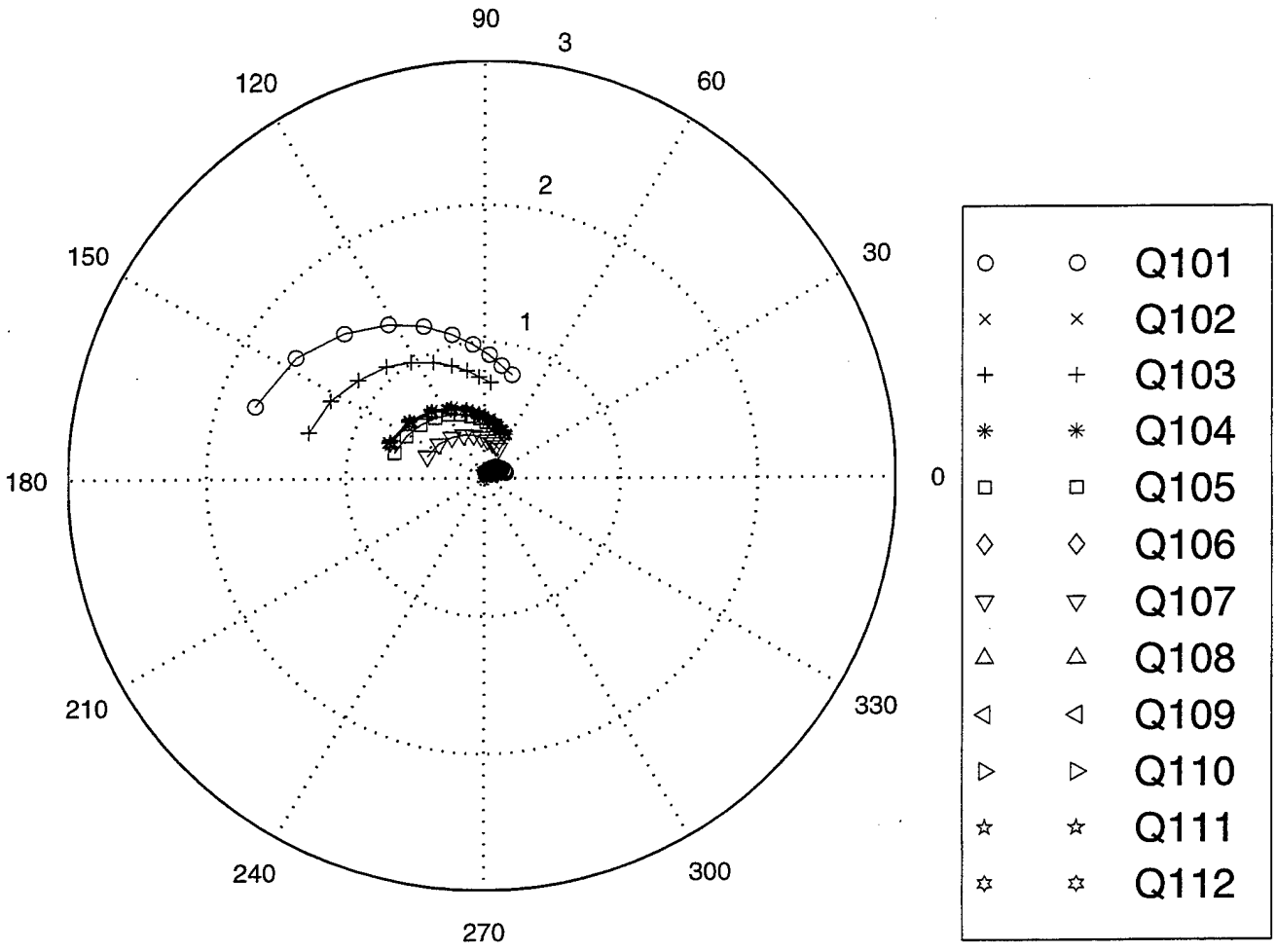

Measured S12 and S21 (Die 6E): Id = 25 mA
90
3
120
60
2
150
30
1
180
0
210
330
240
300
270
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

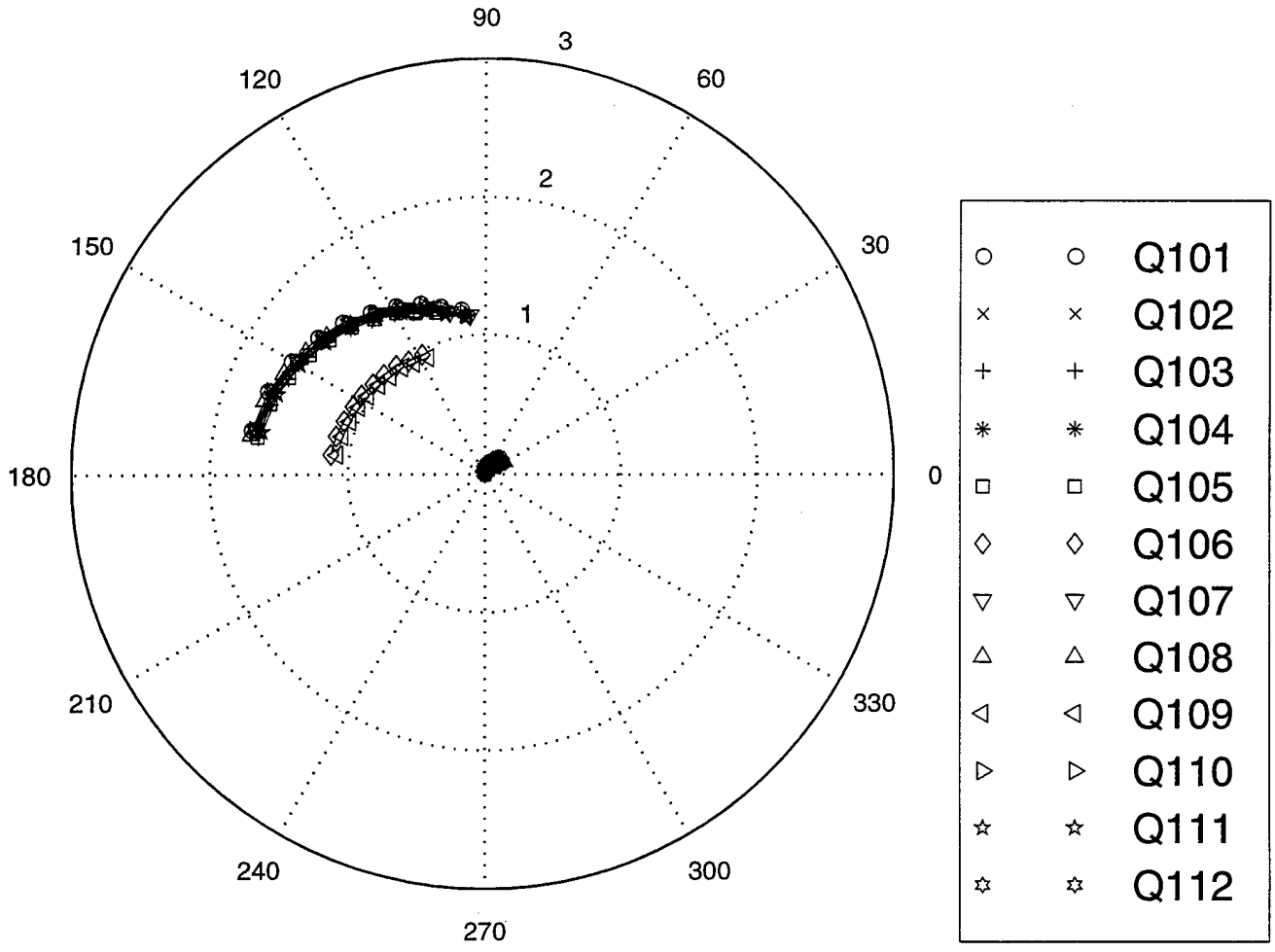

Measured S12 and S21 (Die 6E): Id = 50 mA
90
3
120
60
2
150
30
1
180
0
210
330
240
300
270
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

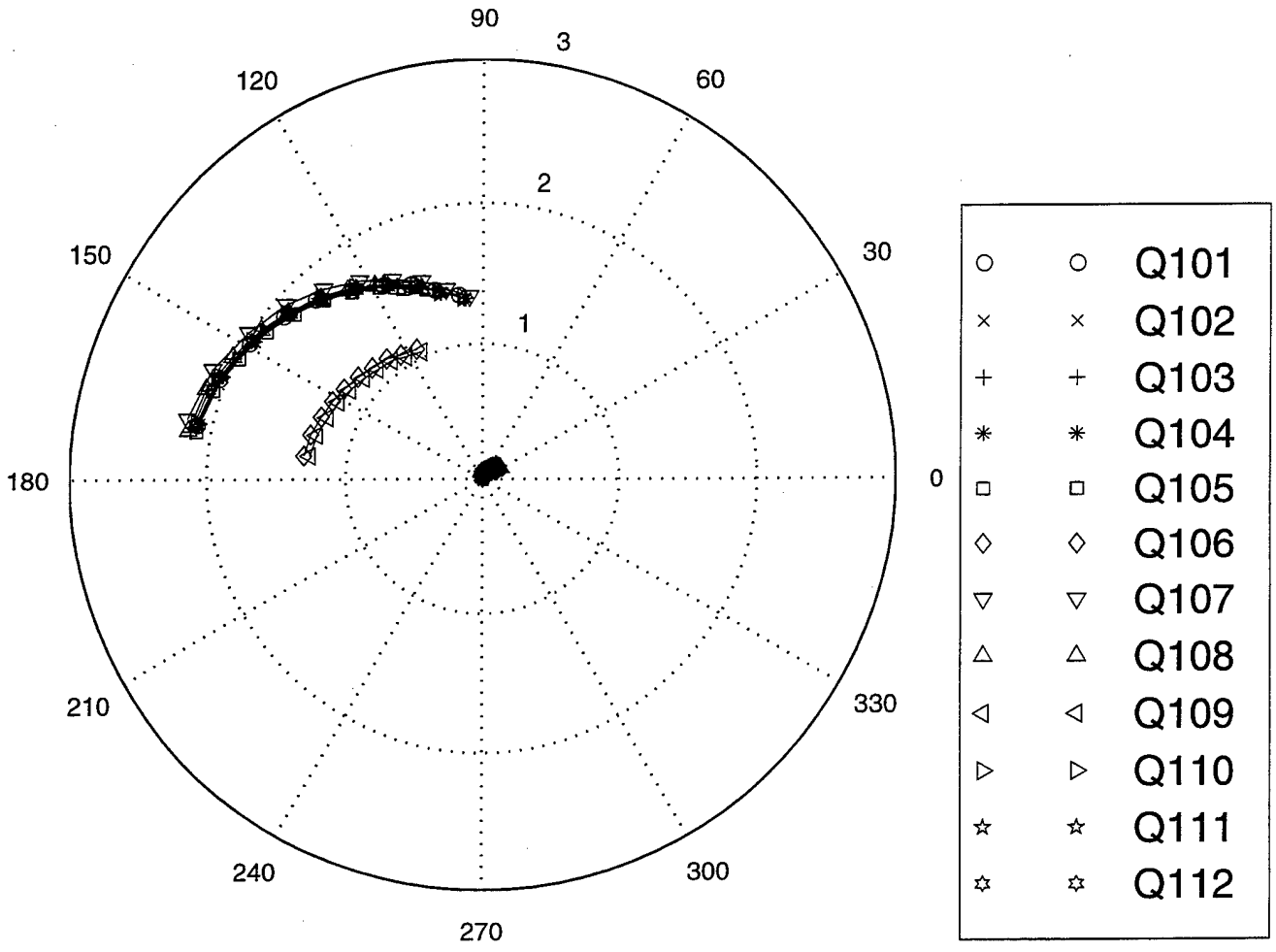
Measured S12 and S21 (Die 6E): Id = 75 mA

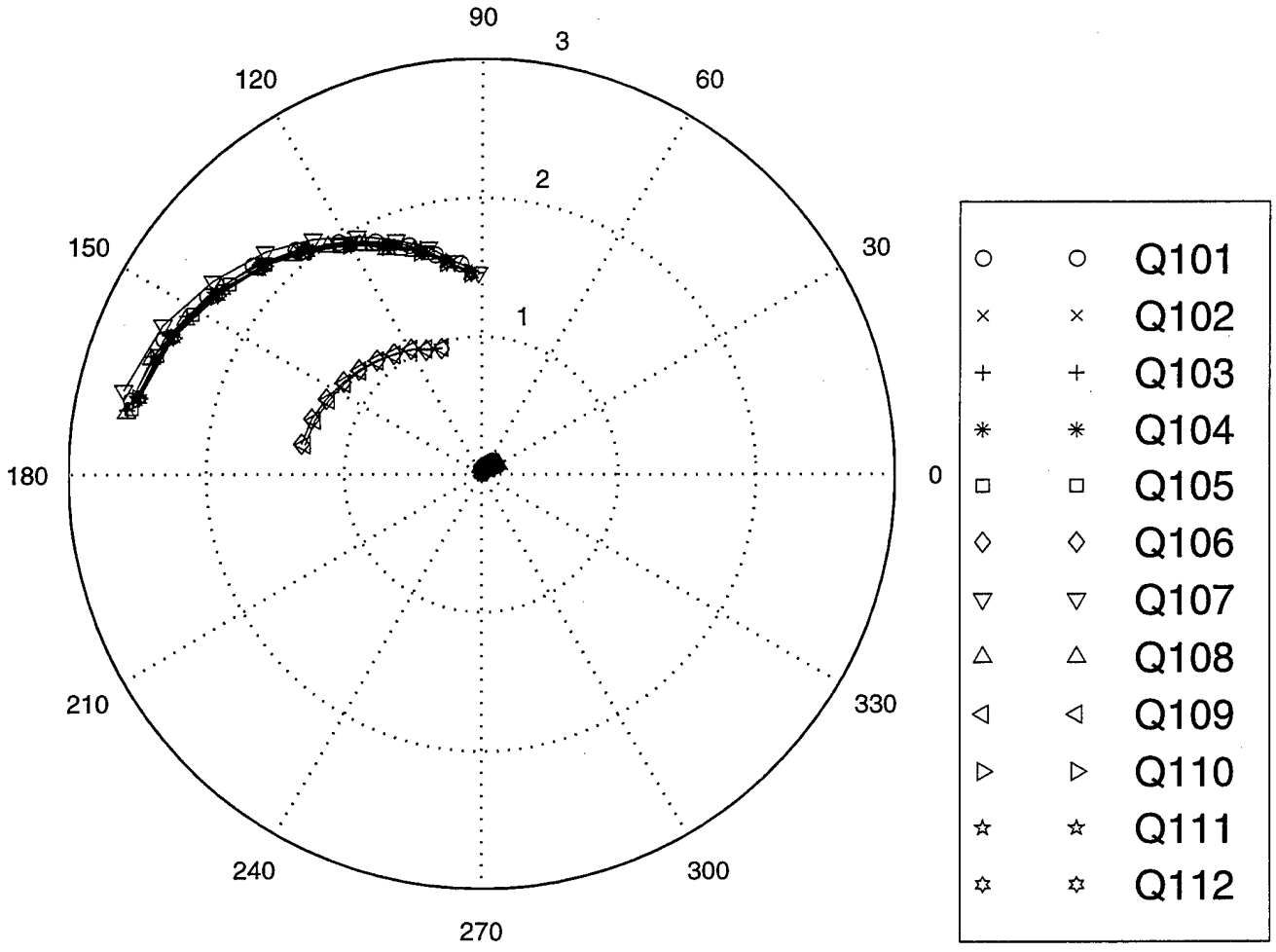


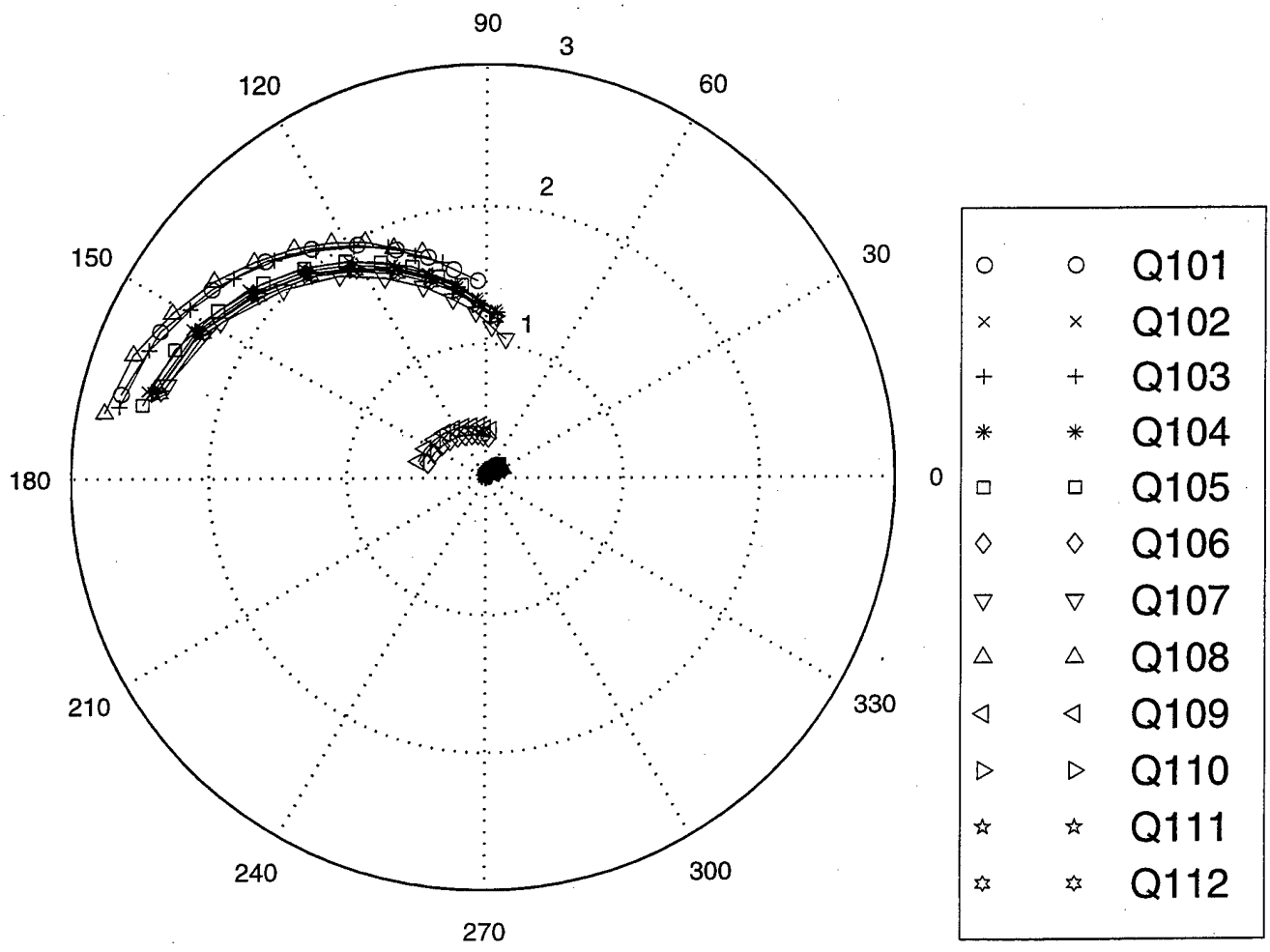
Measured S12 and S21 (Die 6E): Id = 100 mA

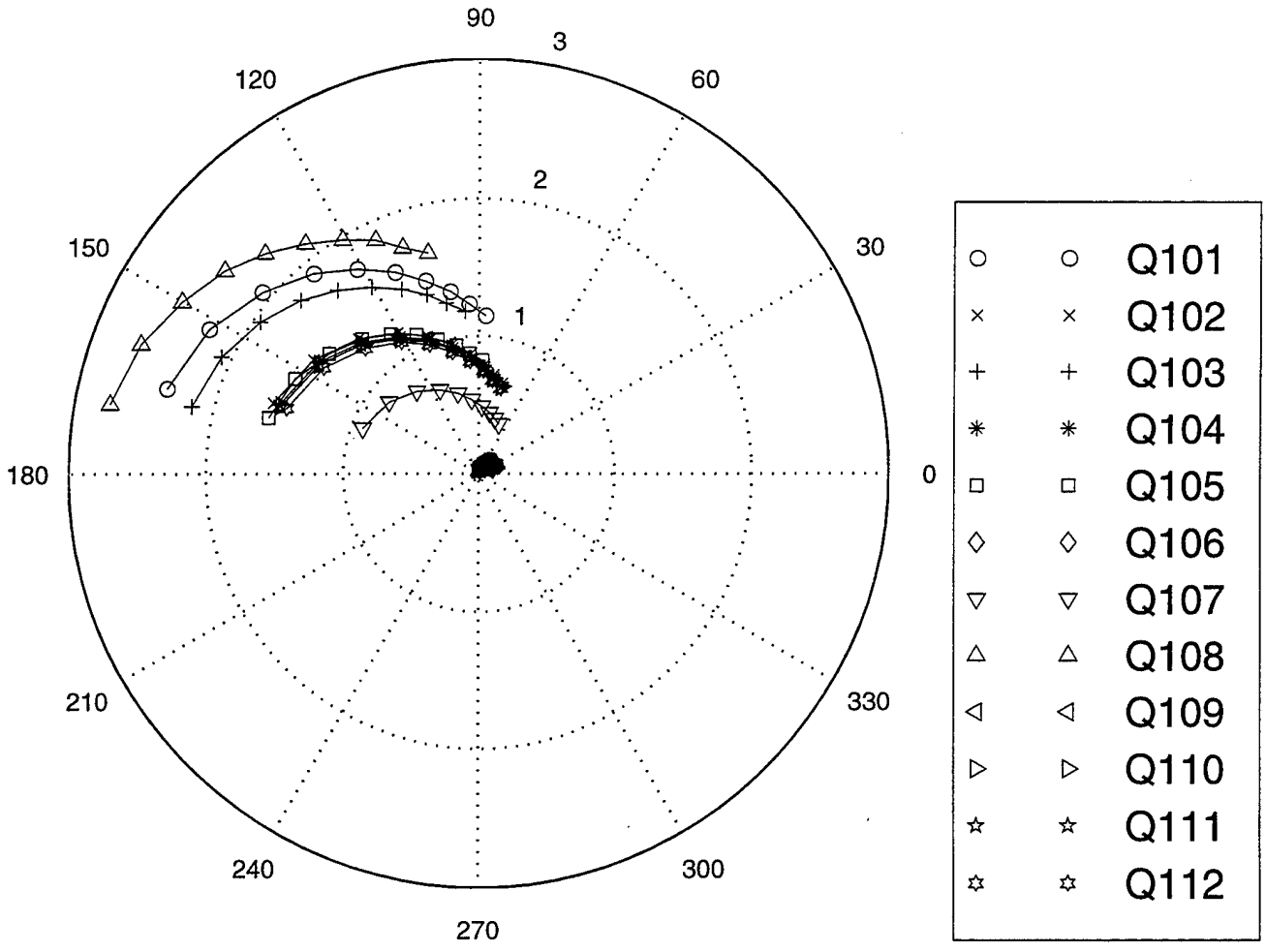



Measured S12 and S21 (Die 8J): Id = 5 mA
90
3
120
60
2
150
30
1
180
0
210
330
240
300
270
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

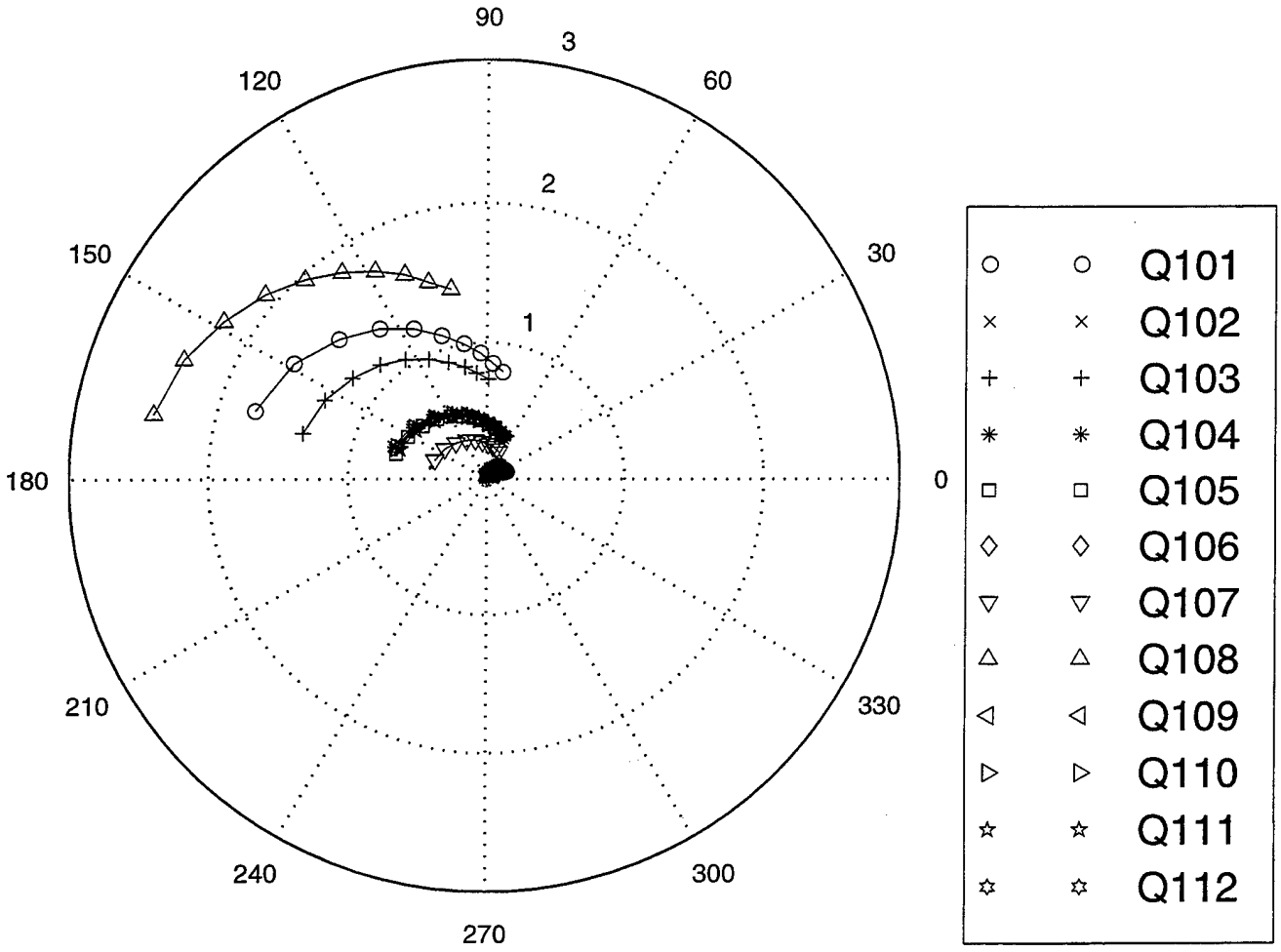

Measured S12 and S21 (Die 8J): Id = 10 mA
90
3
120
60
2
150
30
1
180
0
210
330
240
300
270
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

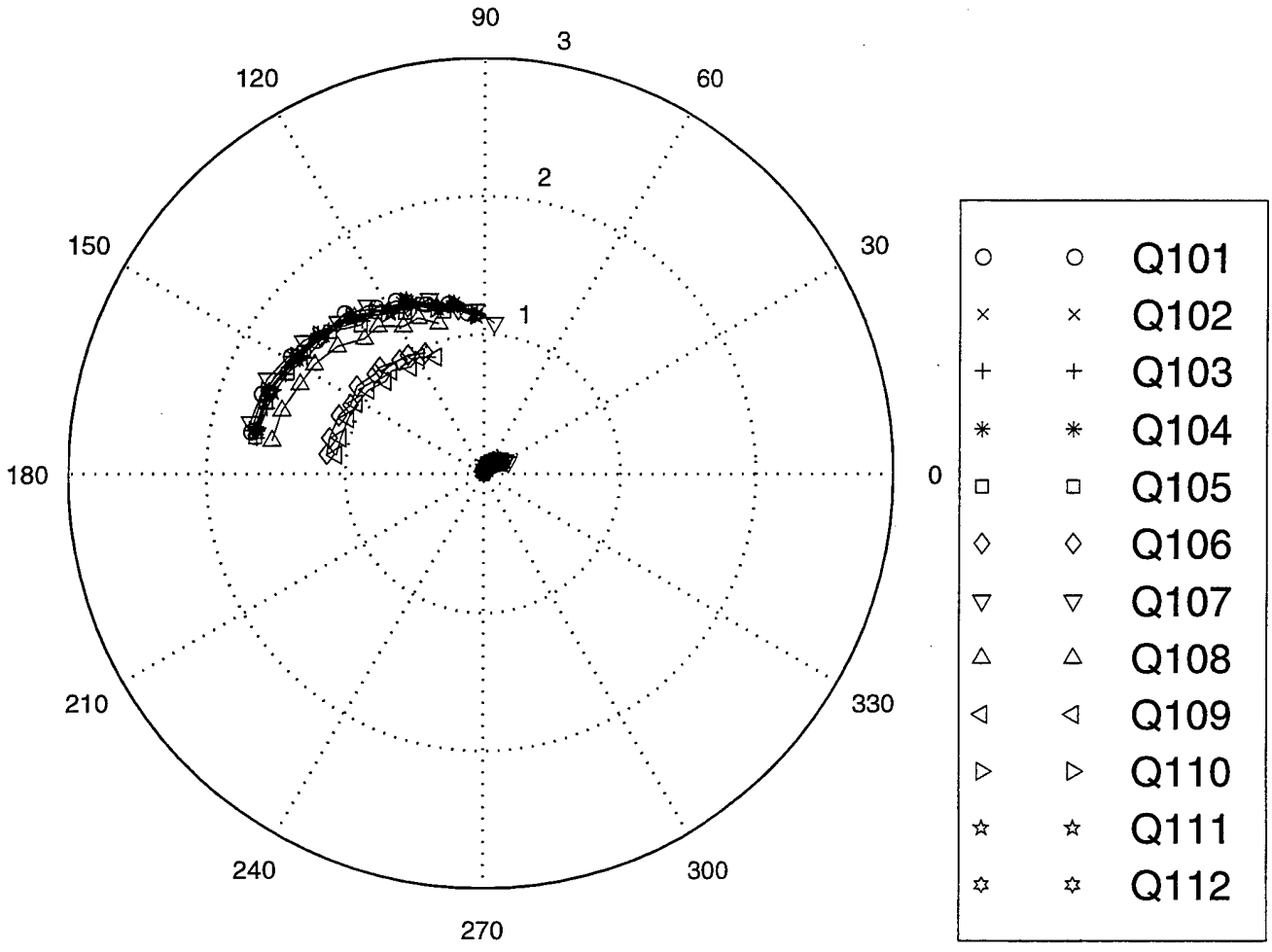

Measured S12 and S21 (Die 8J): Id = 25 mA
90
3
120
60
2
150
30
1
180
0
210
330
240
300
270
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112


Measured S12 and S21 (Die 8J): Id = 50 mA
90
3
120
60
2
150
30
1
180
0
210
330
240
300
270
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

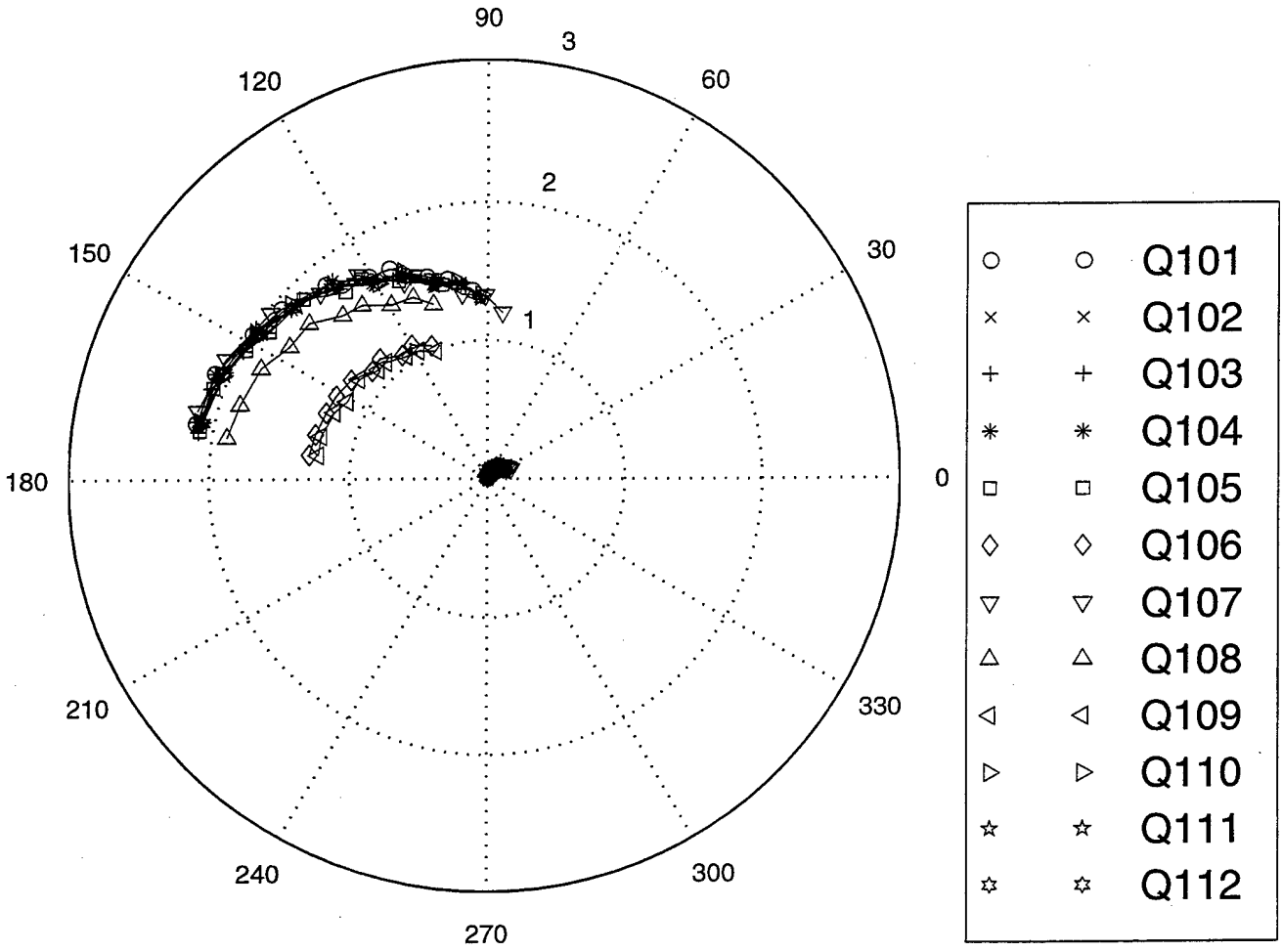

Measured S12 and S21 (Die 8J): Id = 75 mA
90
3
120
60
2
150
30
1
180
0
210
330
240
300
270
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

Measured S12 and S21 (Die 8J): Id = 100 mA

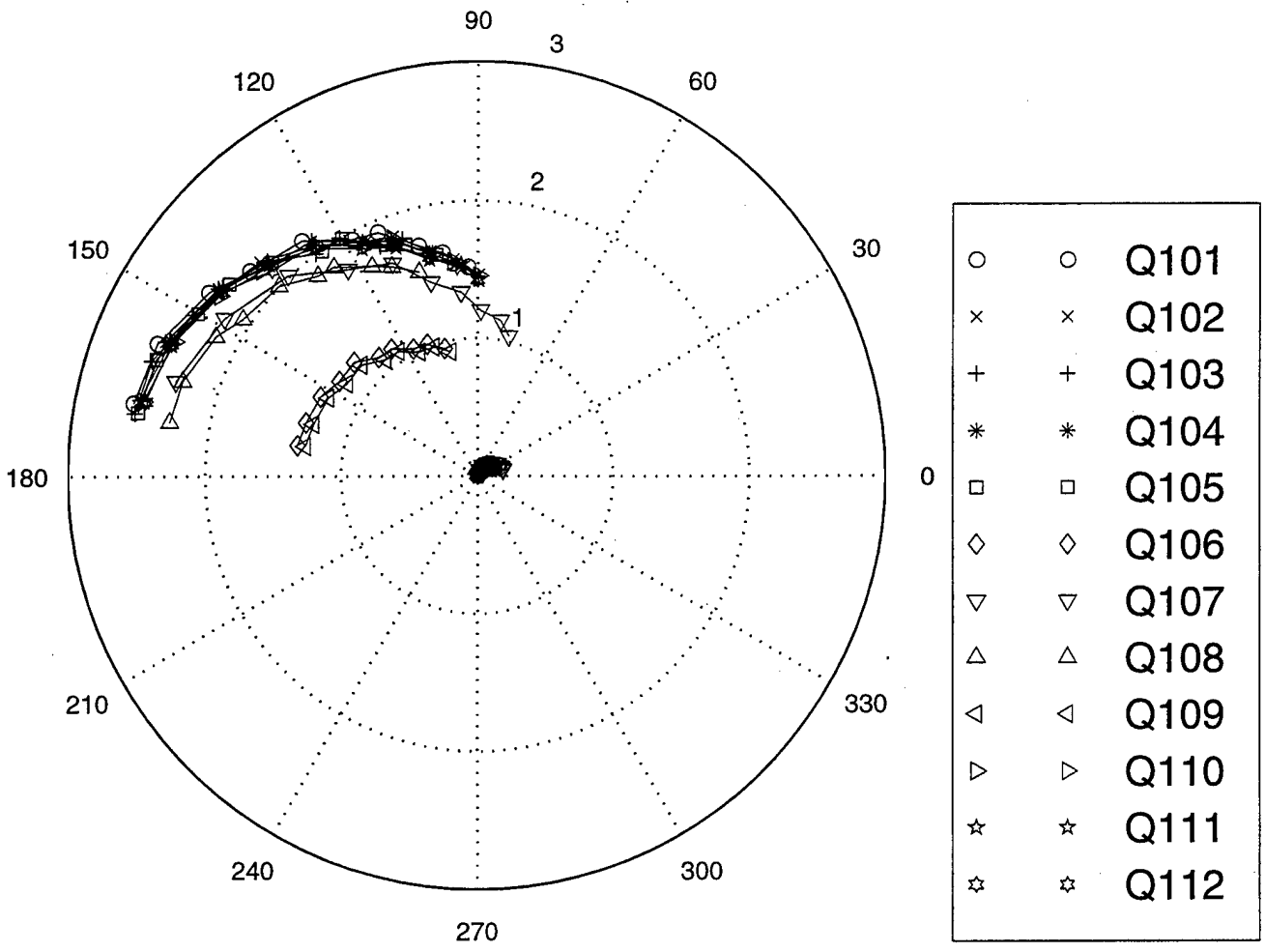



Measured S12 and S21 (Die 13O): Id = 5 mA
90
3
120
60
2
150
30
1
180
0
210
330
240
300
270
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

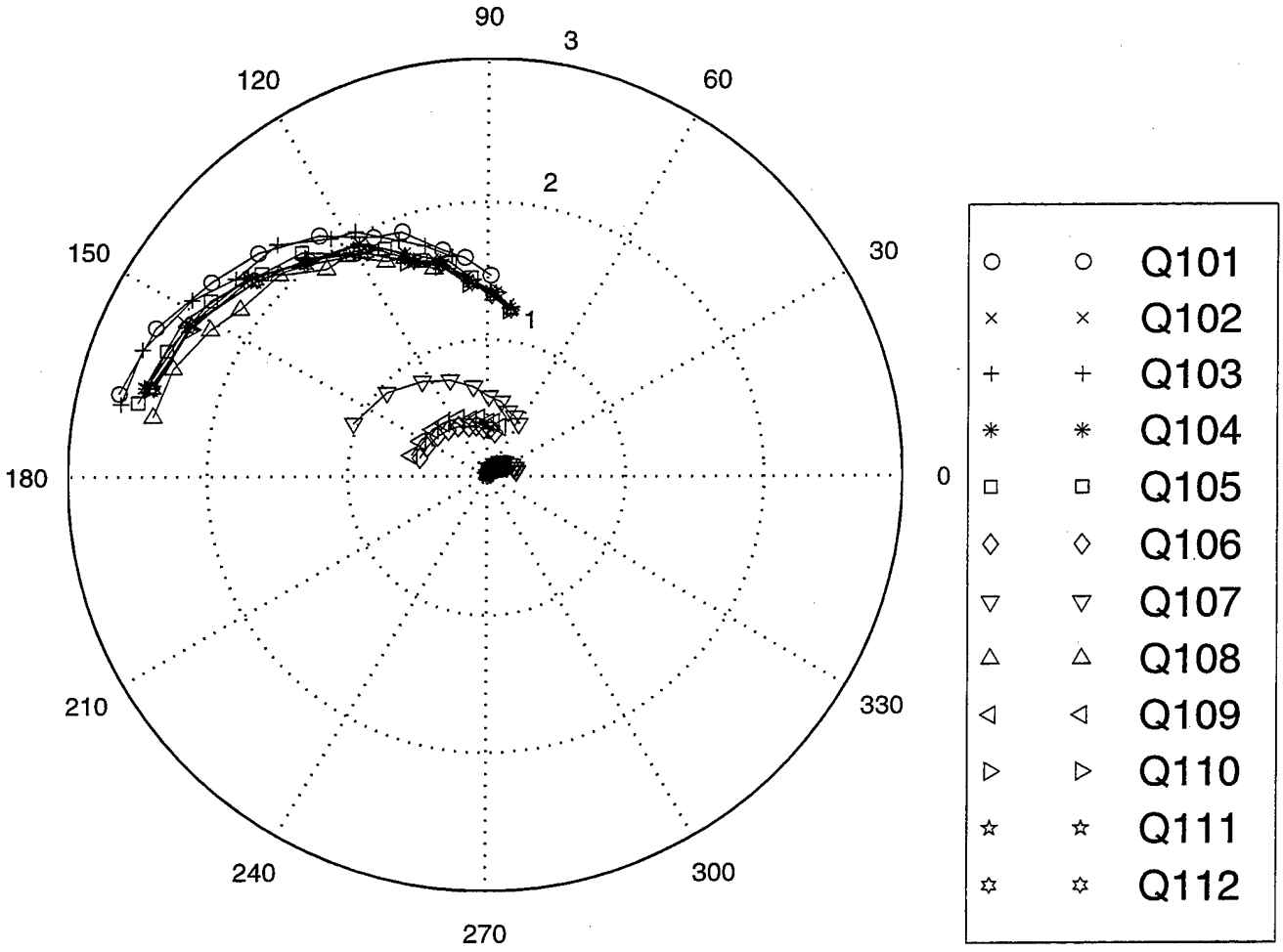
Measured S12 and S21 (Die 13O): Id = 10 mA



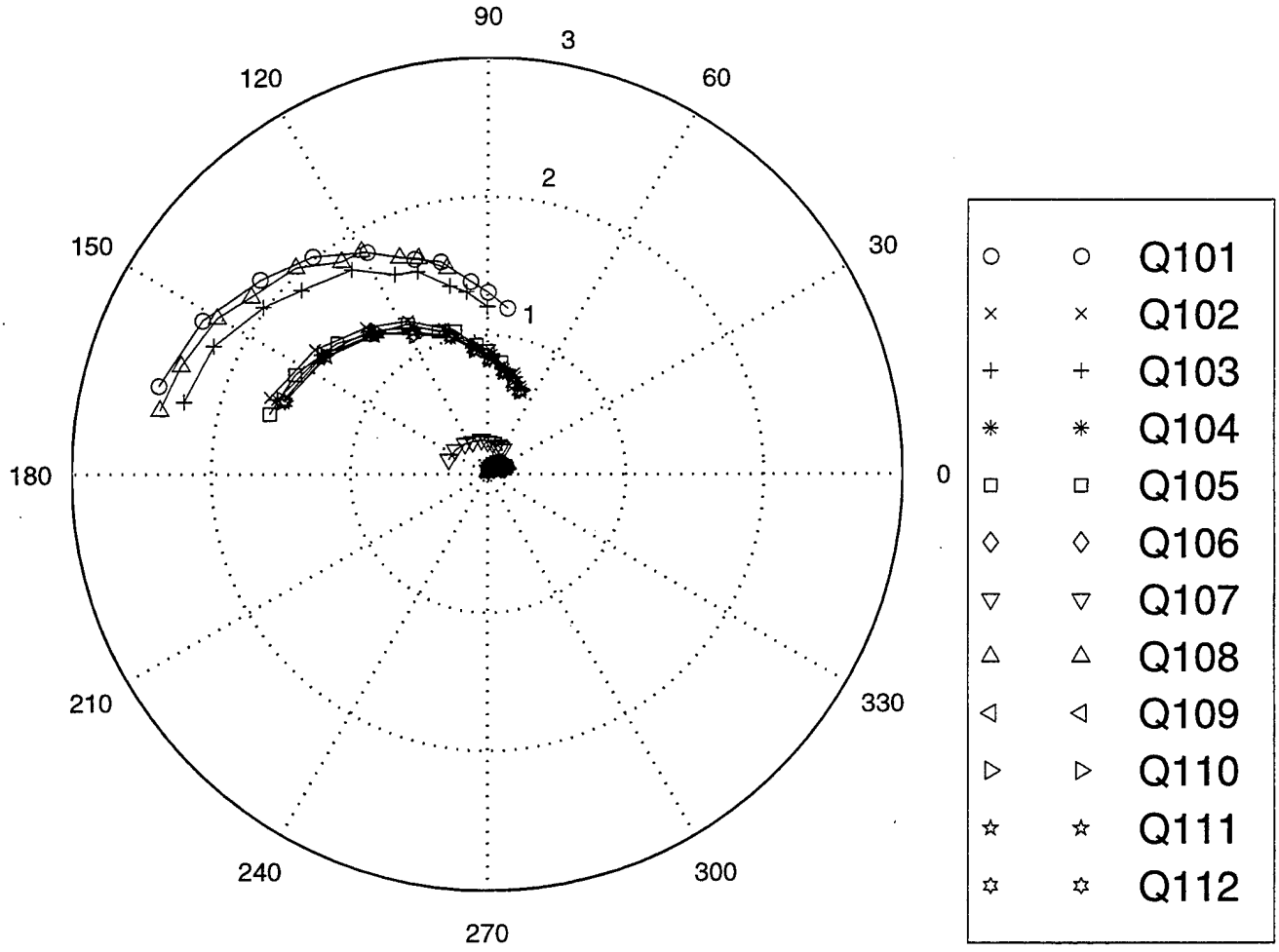
Measured S12 and S21 (Die 13O): Id = 25 mA



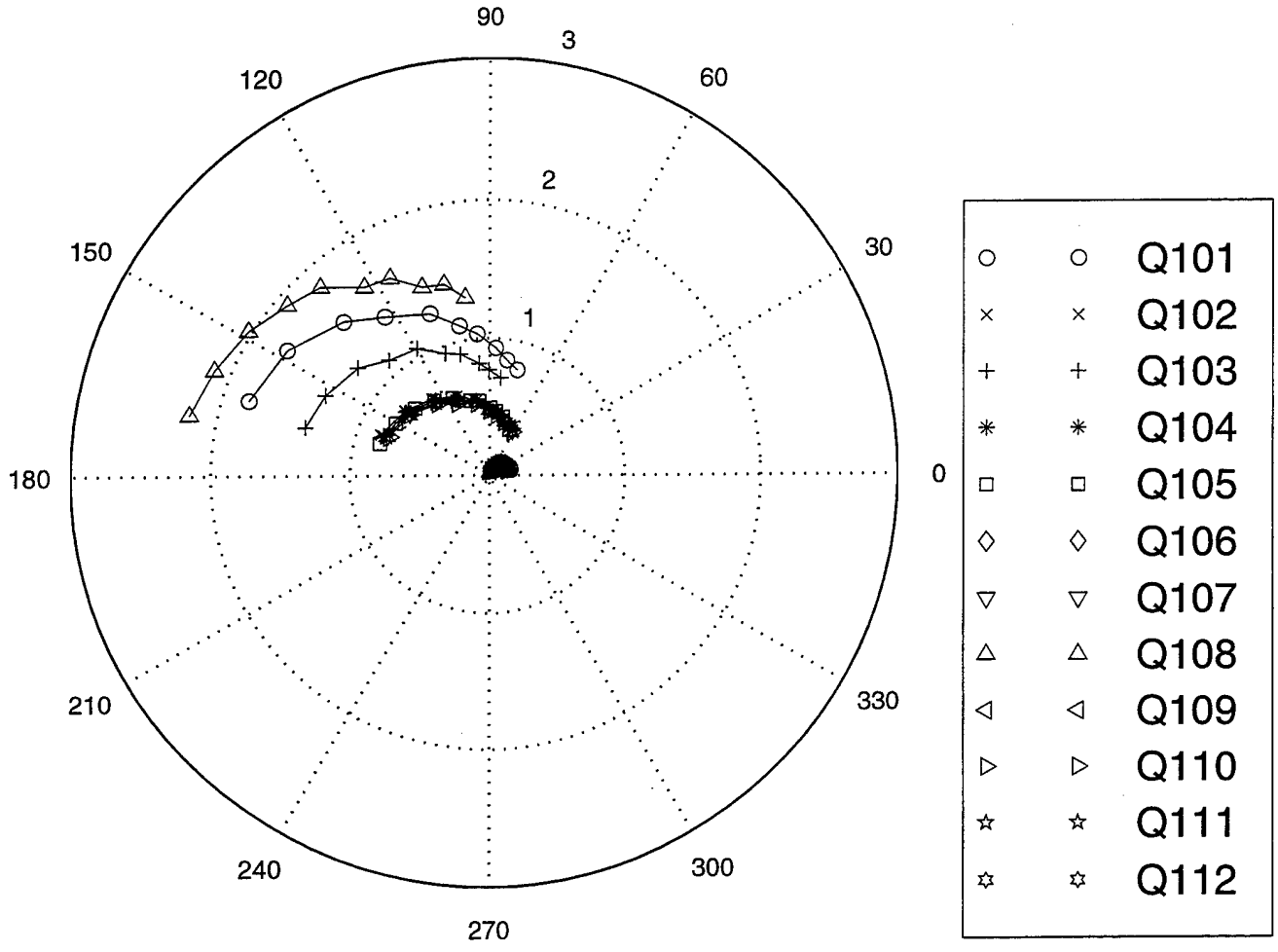
Measured S12 and S21 (Die 13O): Id = 50 mA

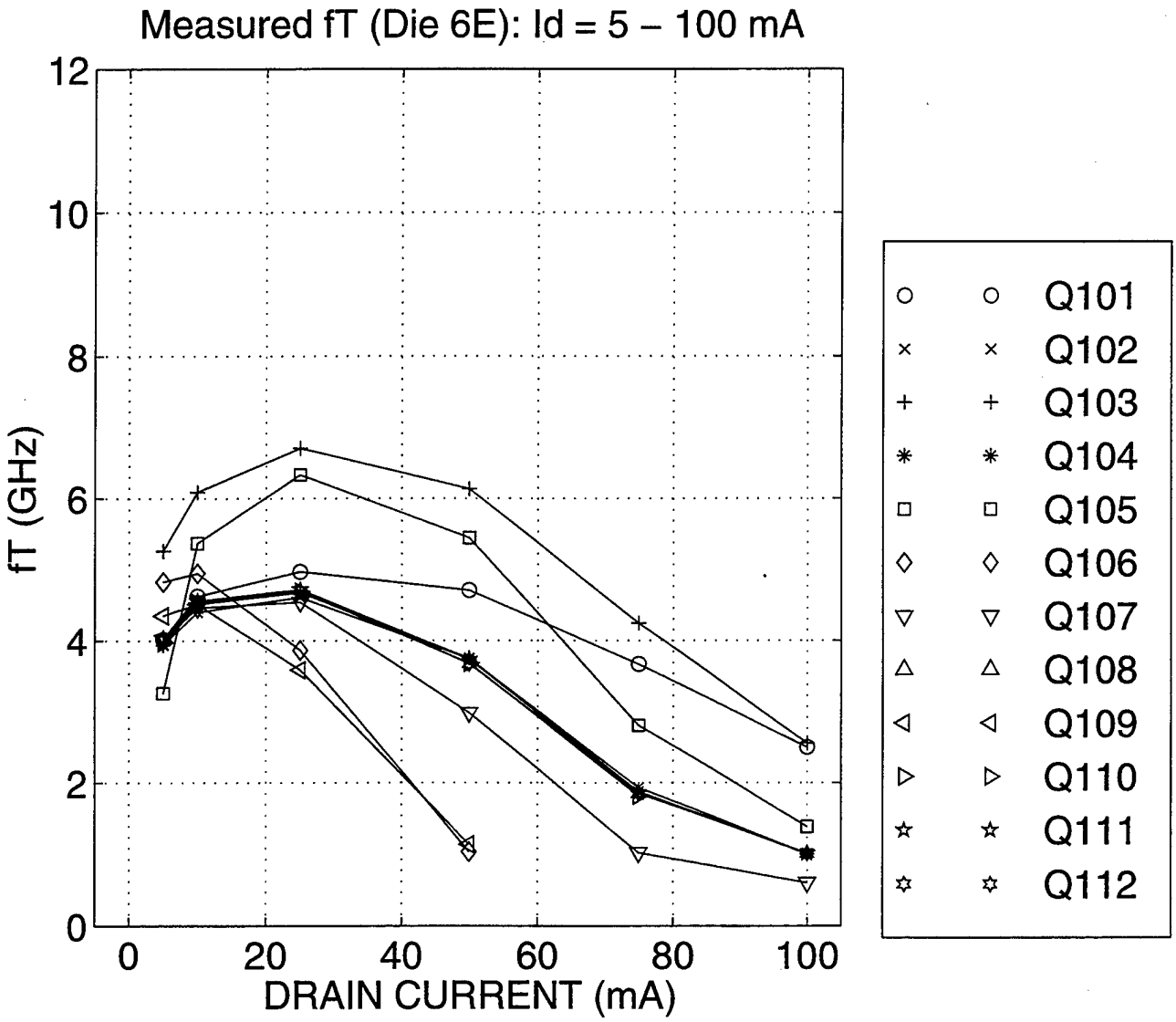


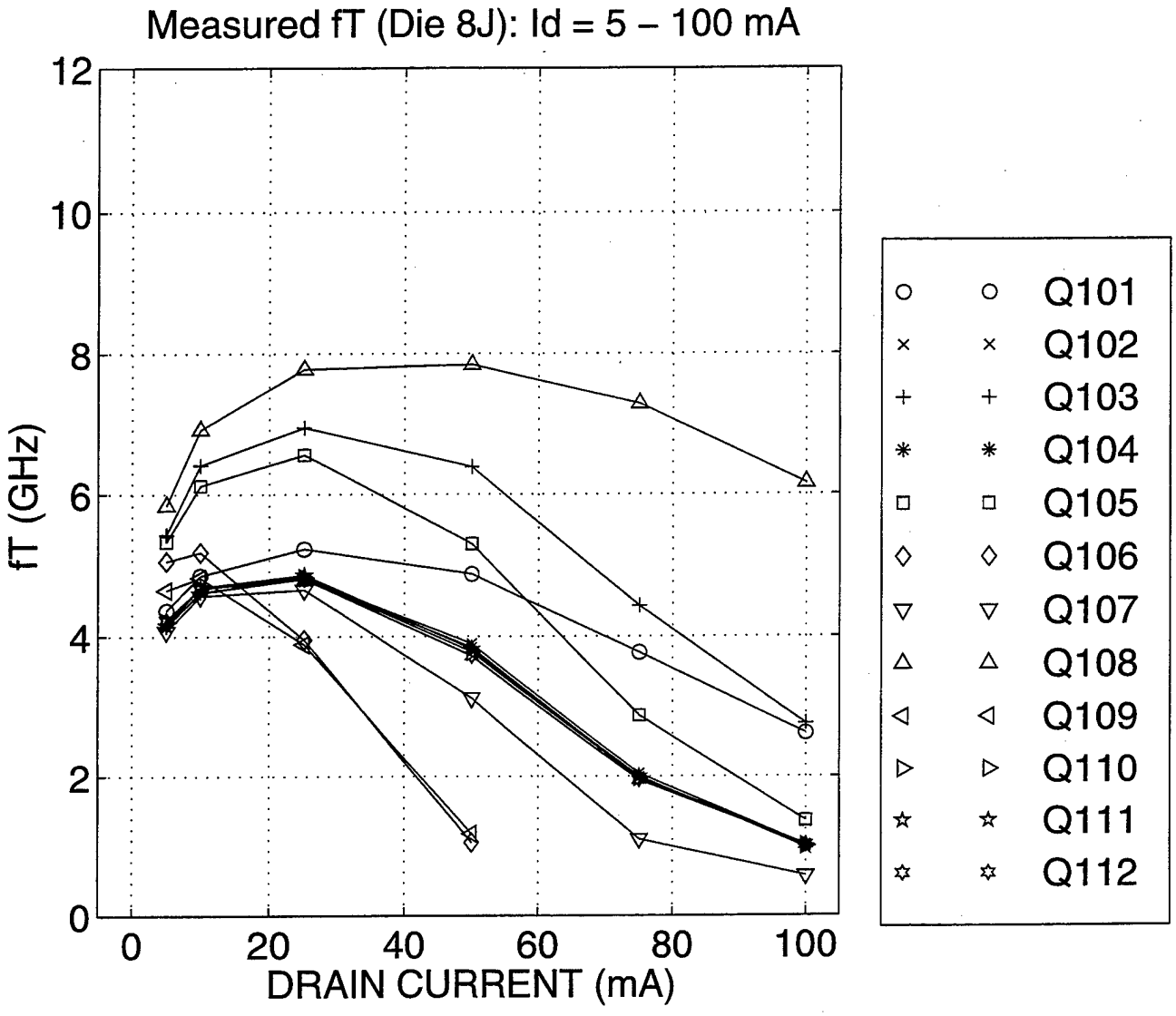
Measured S12 and S21 (Die 13O): Id = 75 mA

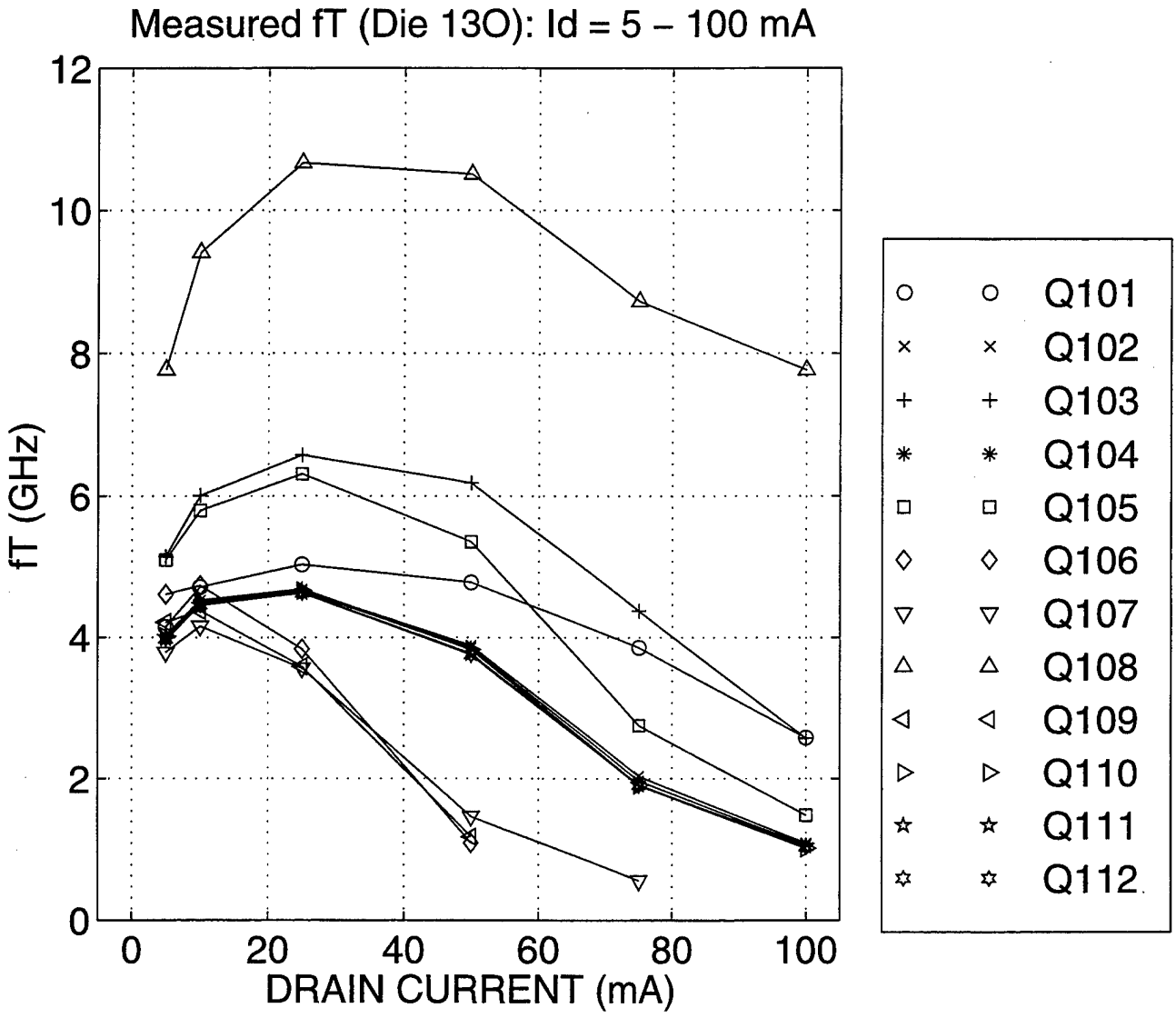


Measured S12 and S21 (Die 13O): Id = 100 mA




Measured fT (Die 6E): Id = 5 – 100 mA
fT (GHz)
DRAIN CURRENT (mA)
0
2
4
6
8
10
12
0
20
40
60
80
100
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112


Measured fT (Die 8J): Id = 5 – 100 mA
fT (GHz)
DRAIN CURRENT (mA)
0
2
4
6
8
10
12
0
20
40
60
80
100
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

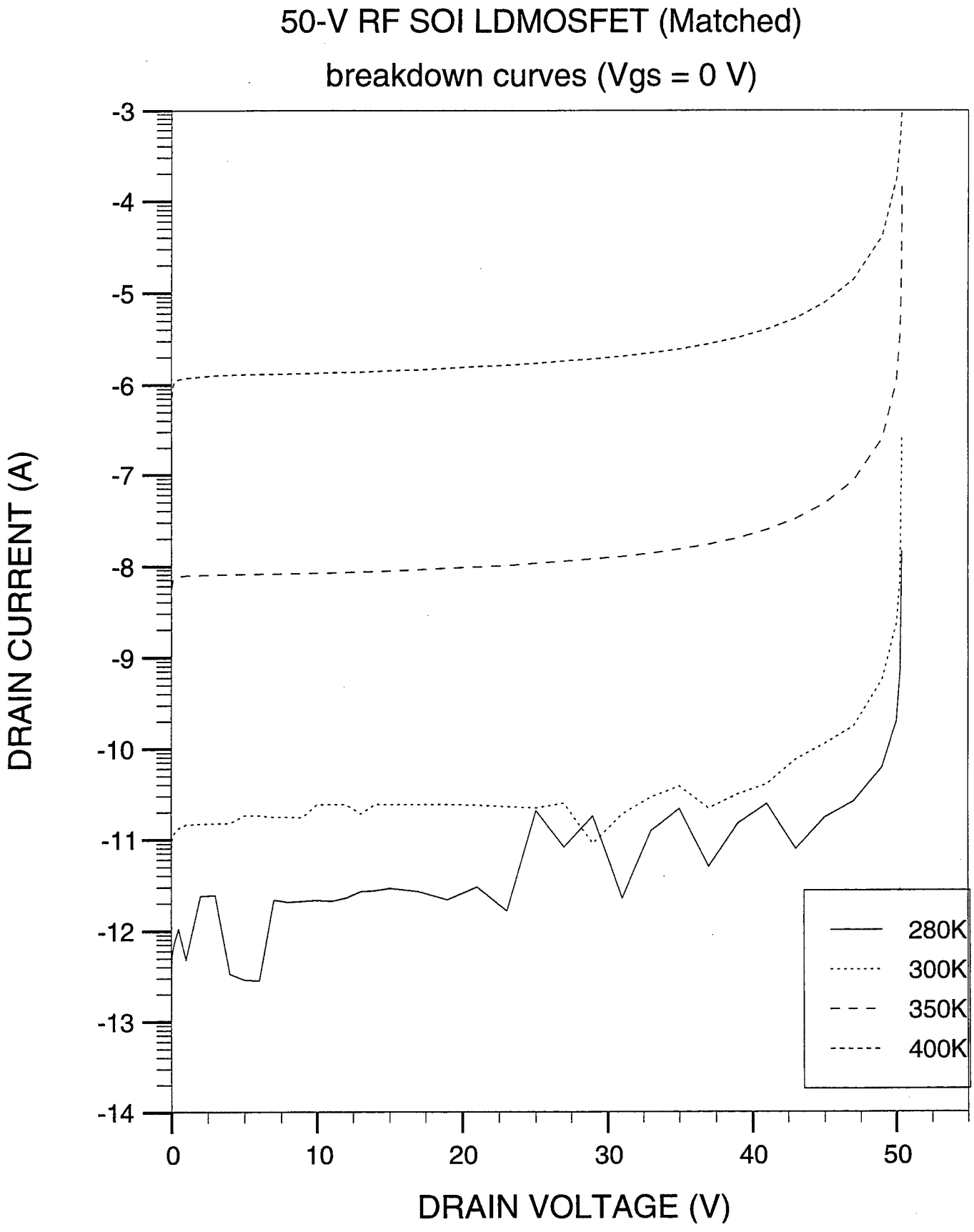

Measured fT (Die 13O): Id = 5 – 100 mA
fT (GHz)
DRAIN CURRENT (mA)
0
2
4
6
8
10
12
0
20
40
60
80
100
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112

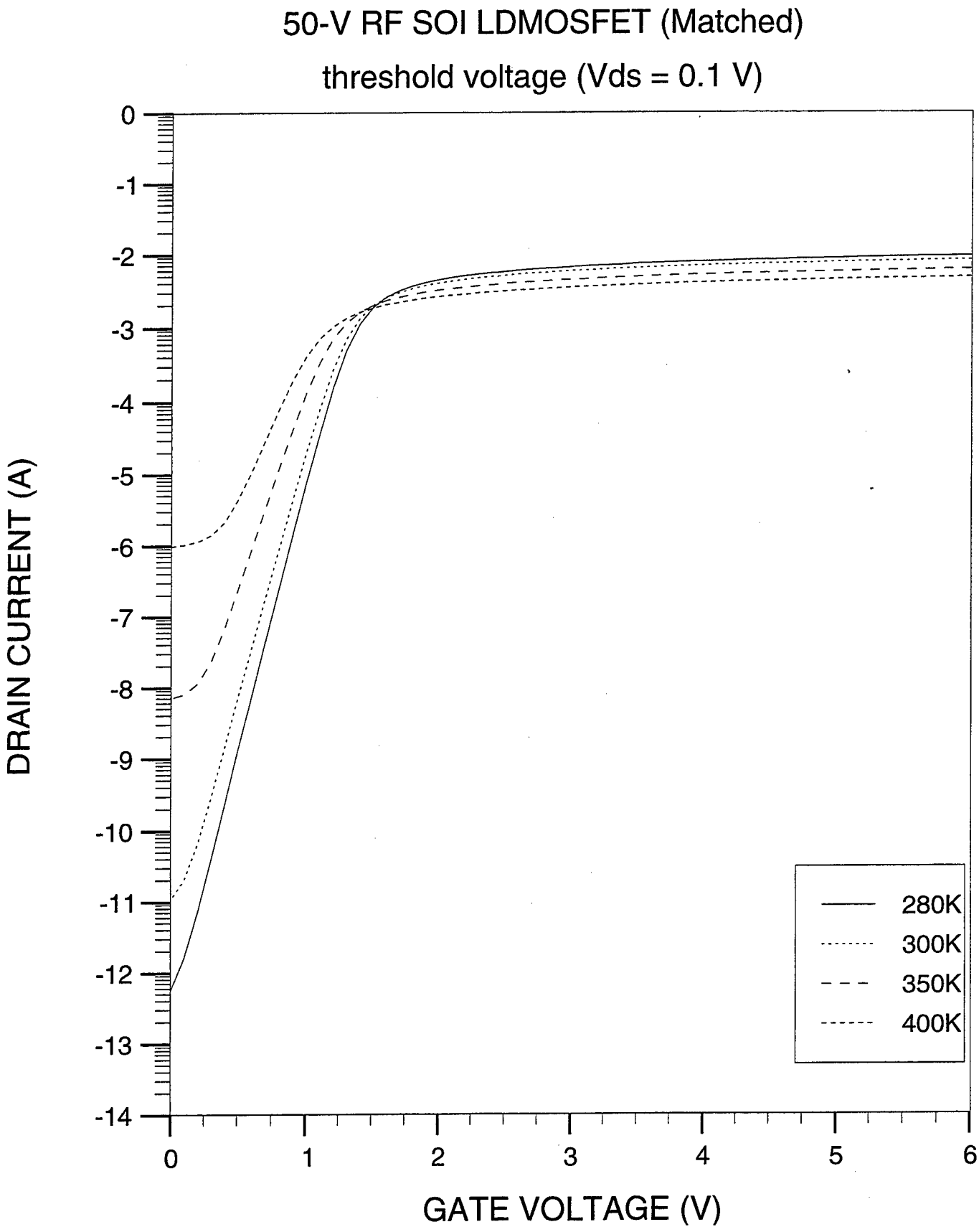
APPENDIX C

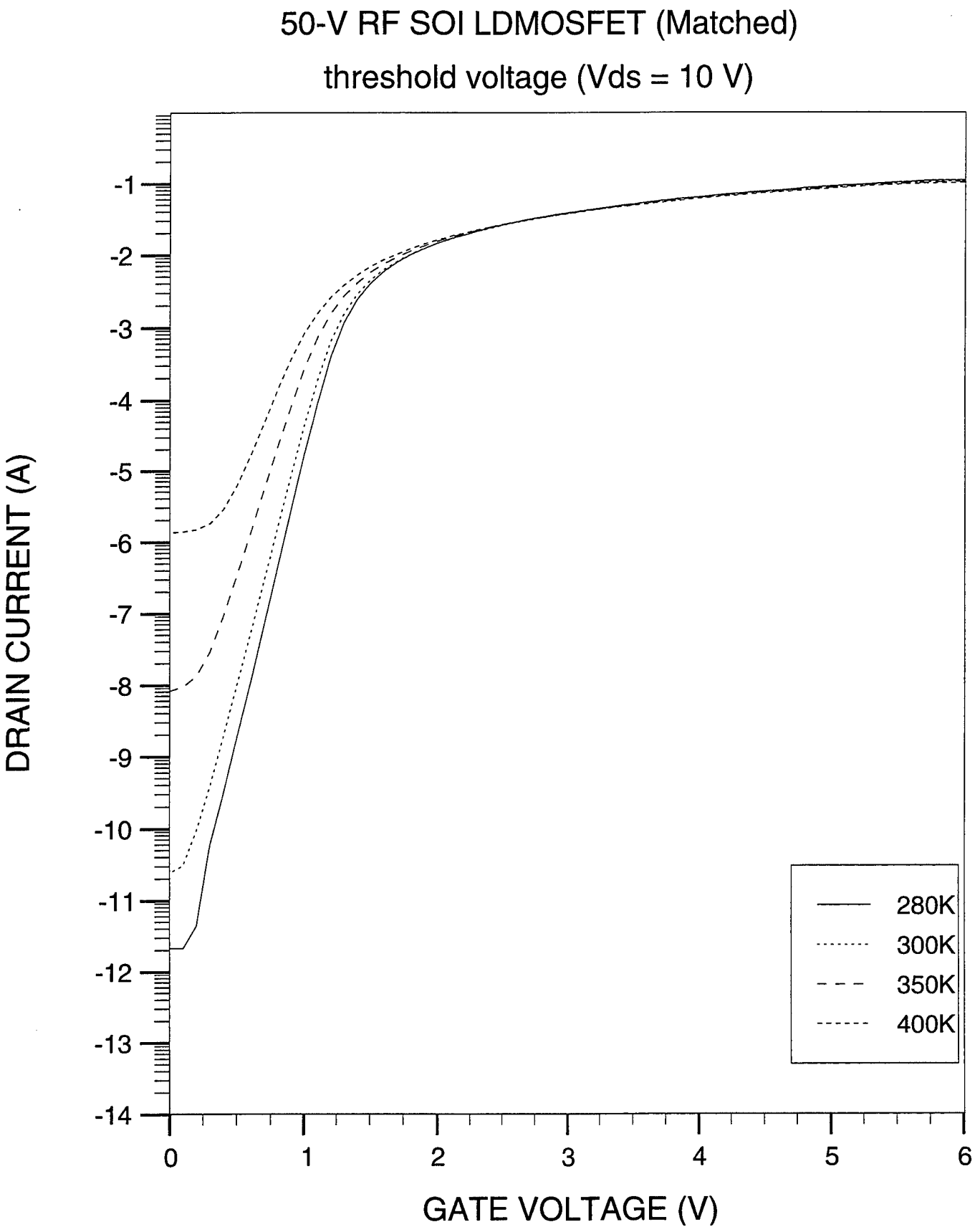
Simulation Data: Matched 2-D Numerical Results of Process and Device Design

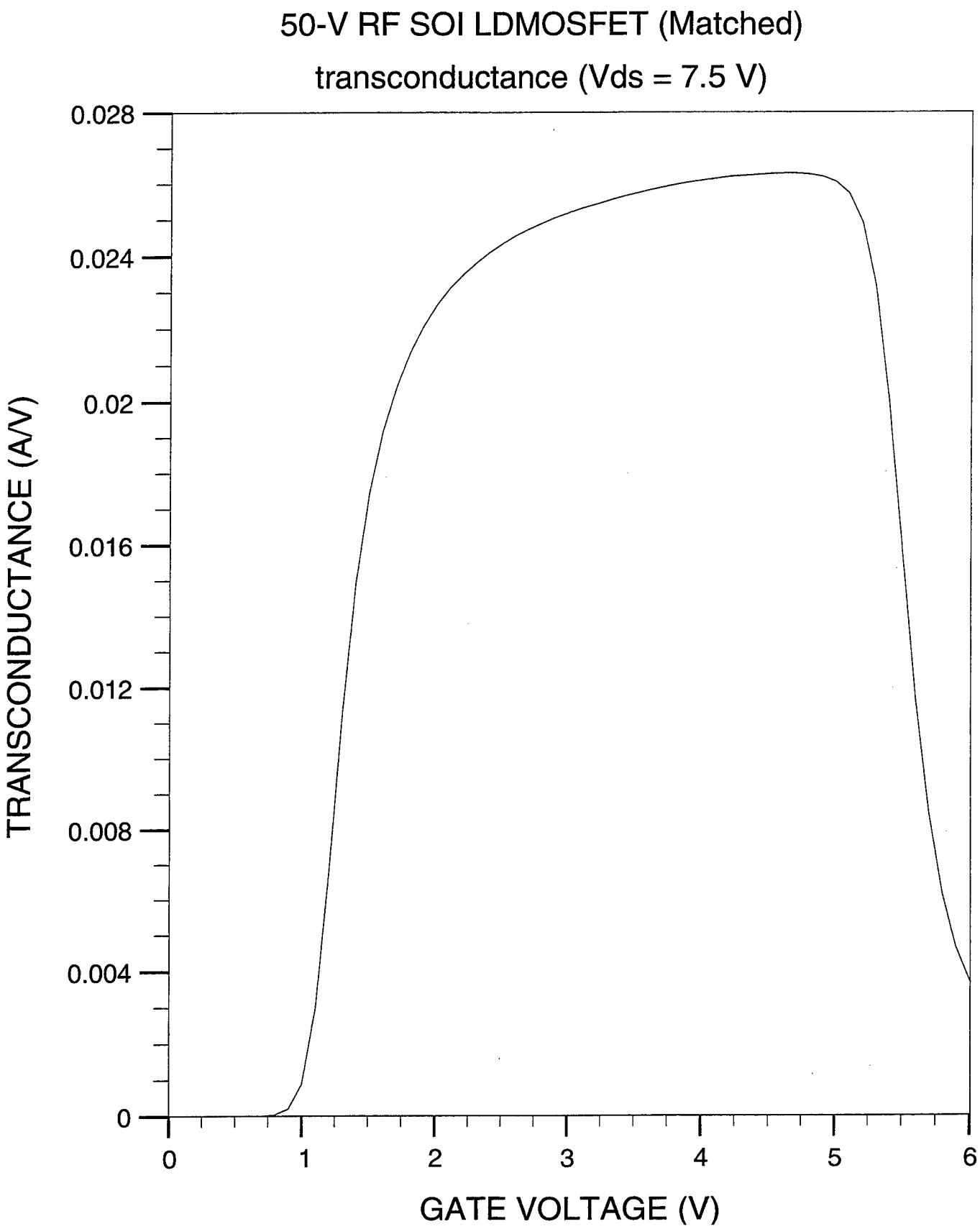
The contents of this section consist of the following waveforms. Bias conditions are noted as appropriate. All 2-D simulations were performed for 280K, 300K, 350K, and 400K.

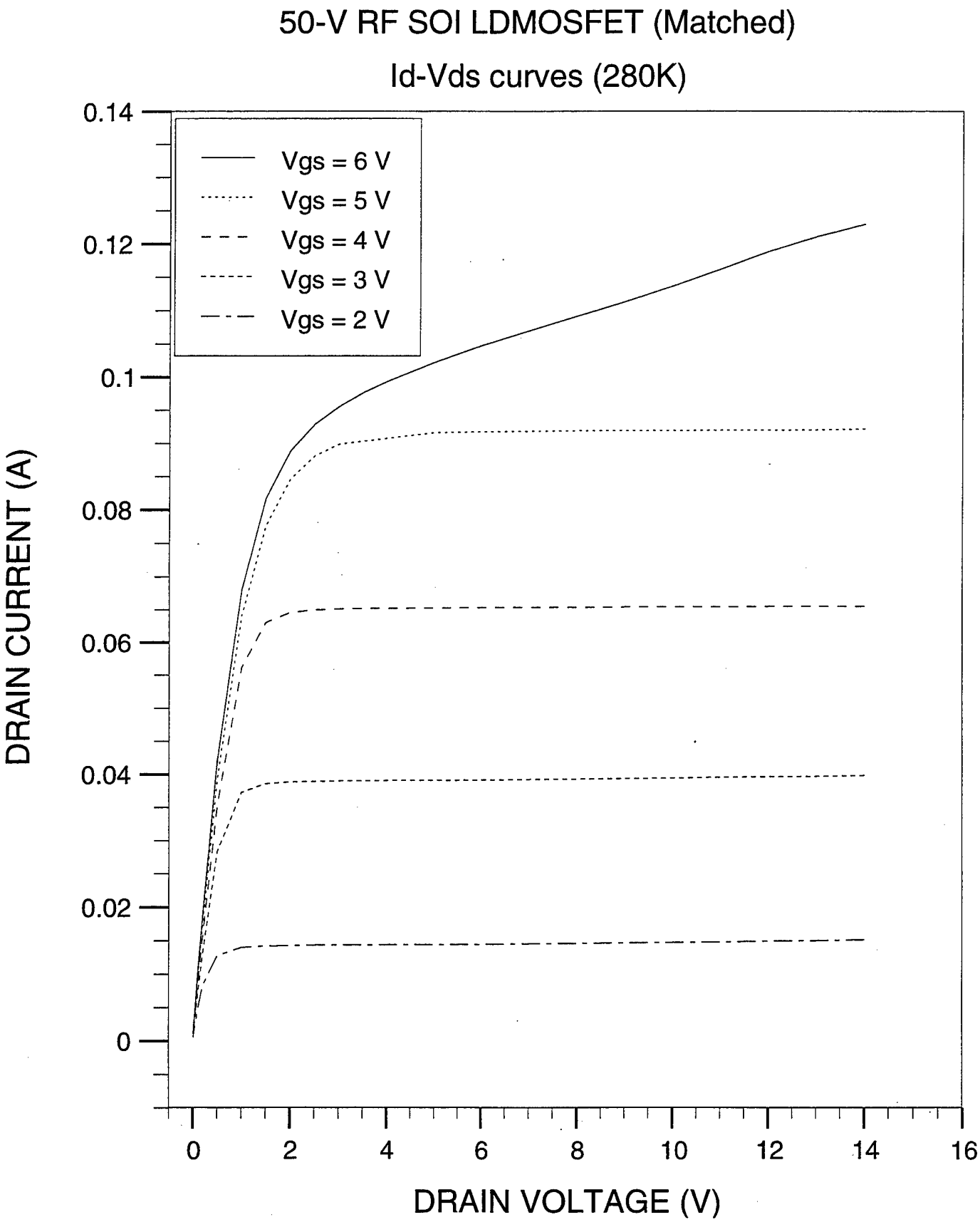
Name	**Conditions**
Drain-source static breakdown (BV_{ds})	V_{gs} = 0 V; V_{ds} = swept
Threshold voltage (V_T)	V_{ds} = 0.1,10 V; V_{gs} = 0–6 V
Transconductance versus gate bias (g_m-V_{gs})	V_{ds} = 7.5 V; V_{gs} = 0–6 V
Maximum transconductance versus drain bias ($g_{m,max}$-V_{ds})	V_{ds} = 2–14 V; V_{gs} = 0–6 V
Forward conduction (I_d-V_{ds})	V_{ds} = 0–18 V; V_{gs} = 2,3,4,5,6 V
Scattering parameters (S_{11} and S_{22})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 10 MHz – 2.9 GHz
Scattering parameters (S_{12} and S_{21})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 10 MHz – 2.9 GHz
Unity current gain frequency versus drain current (f_T-I_d)	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA

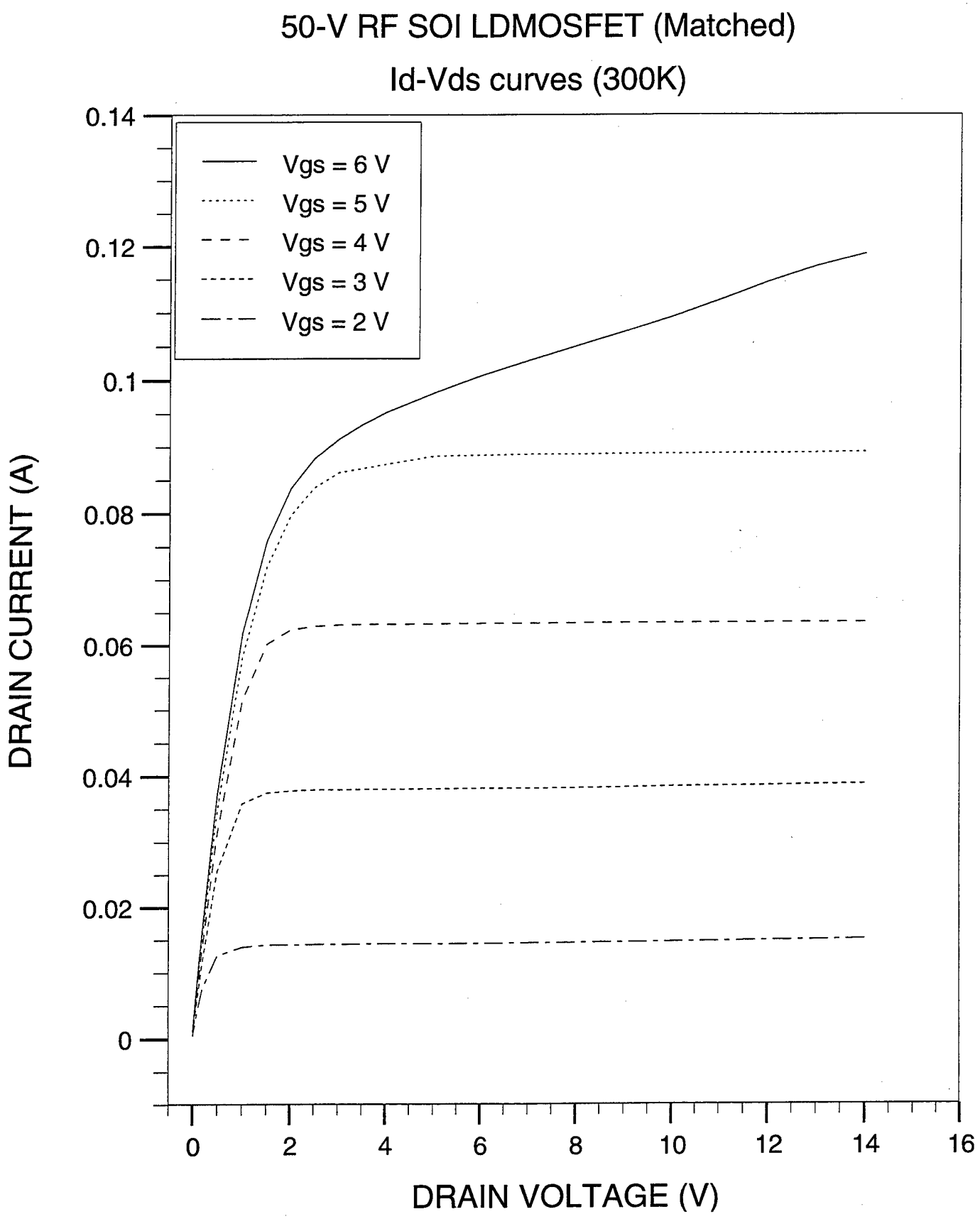

50-V RF SOI LDMOSFET (Matched)
breakdown curves (Vgs = 0 V)
DRAIN CURRENT (A)
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
-14
0
10
20
30
40
50
DRAIN VOLTAGE (V)
280K
300K
350K
400K

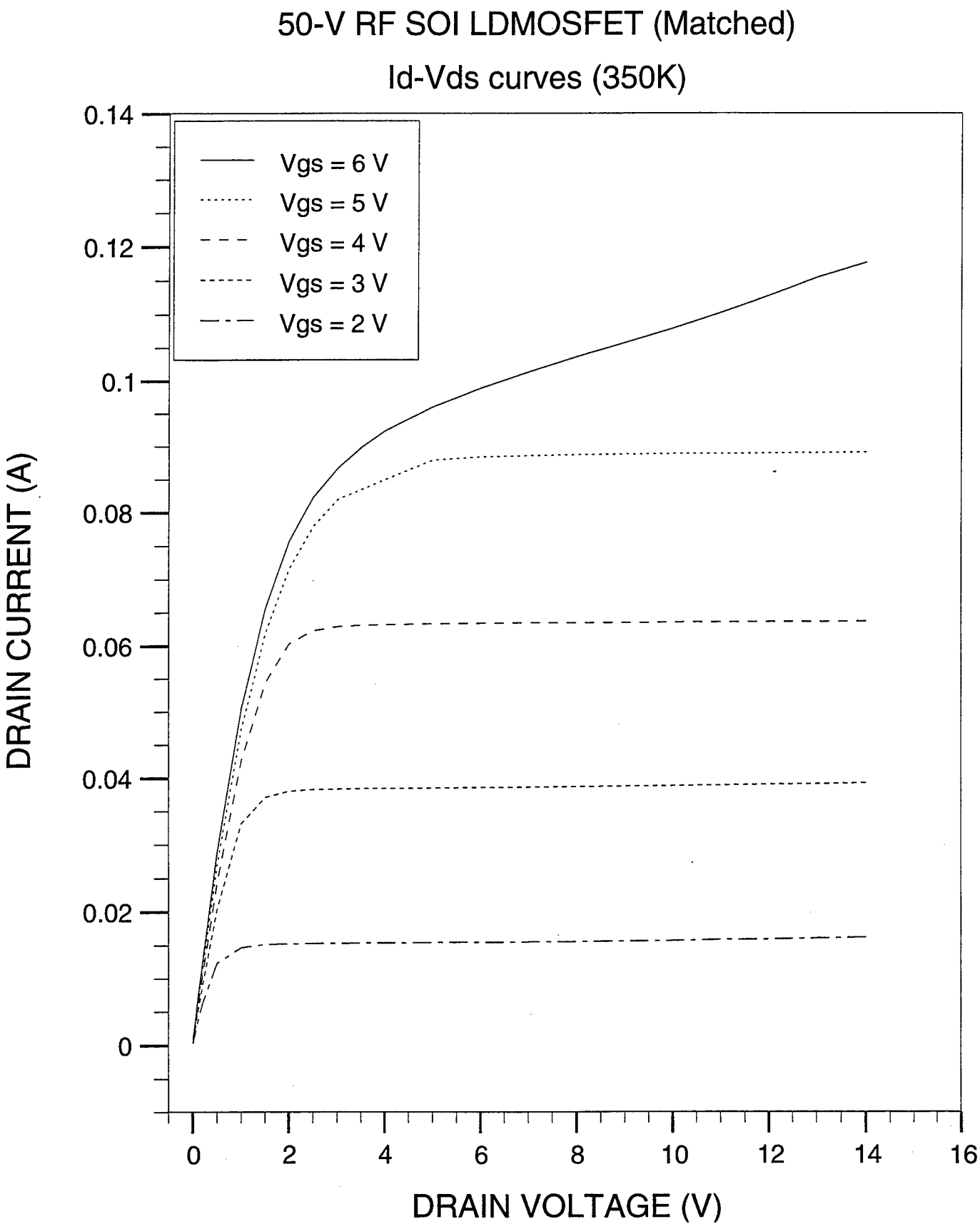

50-V RF SOI LDMOSFET (Matched)
threshold voltage (Vds = 0.1 V)
DRAIN CURRENT (A)
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
-14
0
1
2
3
4
5
6
GATE VOLTAGE (V)
280K
300K
350K
400K

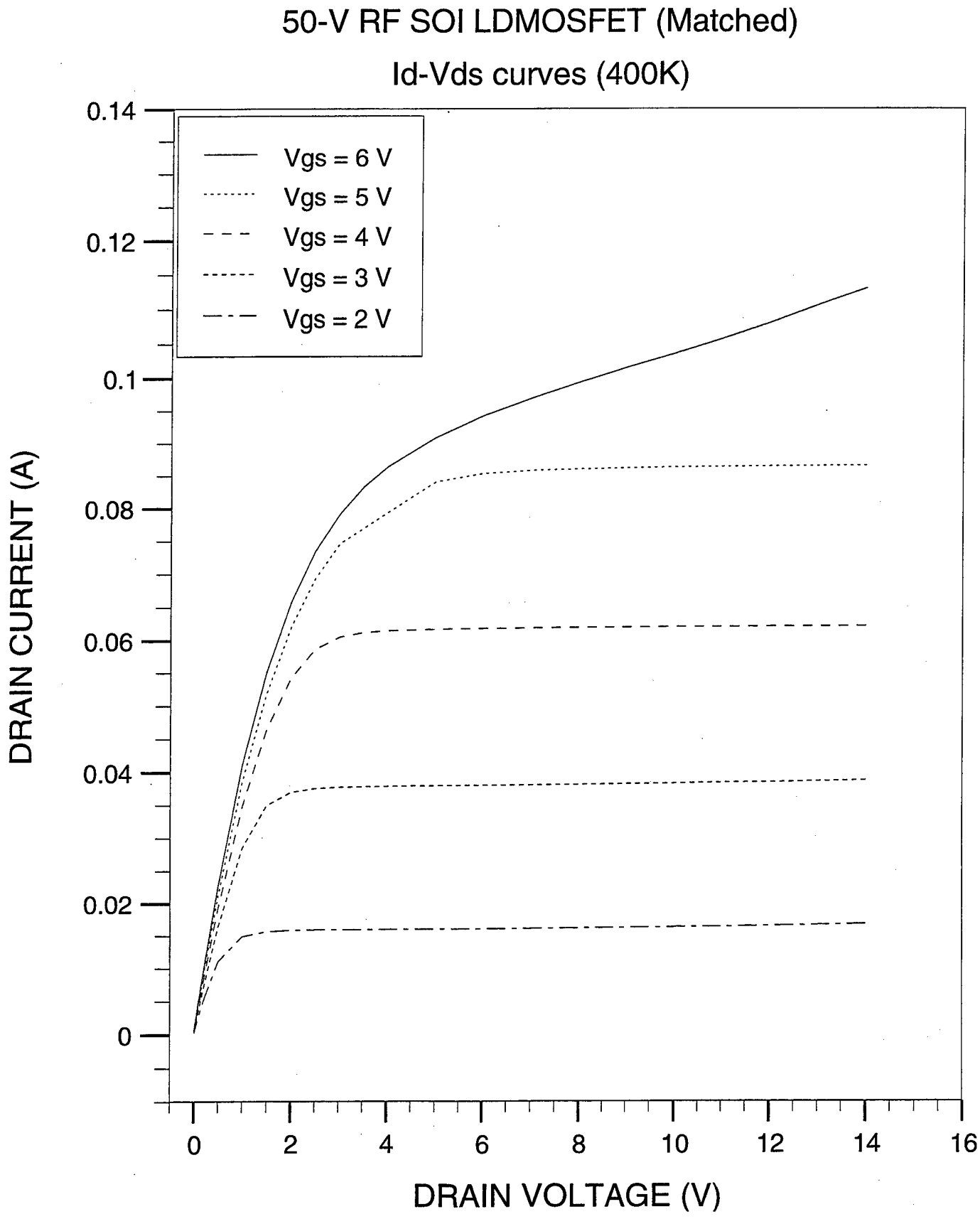

50-V RF SOI LDMOSFET (Matched)
threshold voltage (Vds = 10 V)
DRAIN CURRENT (A)
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
-14
0
1
2
3
4
5
6
GATE VOLTAGE (V)
280K
300K
350K
400K


50-V RF SOI LDMOSFET (Matched)
transconductance (Vds = 7.5 V)
TRANSCONDUCTANCE (A/V)
0.028
0.024
0.02
0.016
0.012
0.008
0.004
0
0
1
2
3
4
5
6
GATE VOLTAGE (V)


50-V RF SOI LDMOSFET (Matched)
Id-Vds curves (280K)
Vgs = 6 V
Vgs = 5 V
Vgs = 4 V
Vgs = 3 V
Vgs = 2 V
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
DRAIN CURRENT (A)
0
2
4
6
8
10
12
14
16
DRAIN VOLTAGE (V)

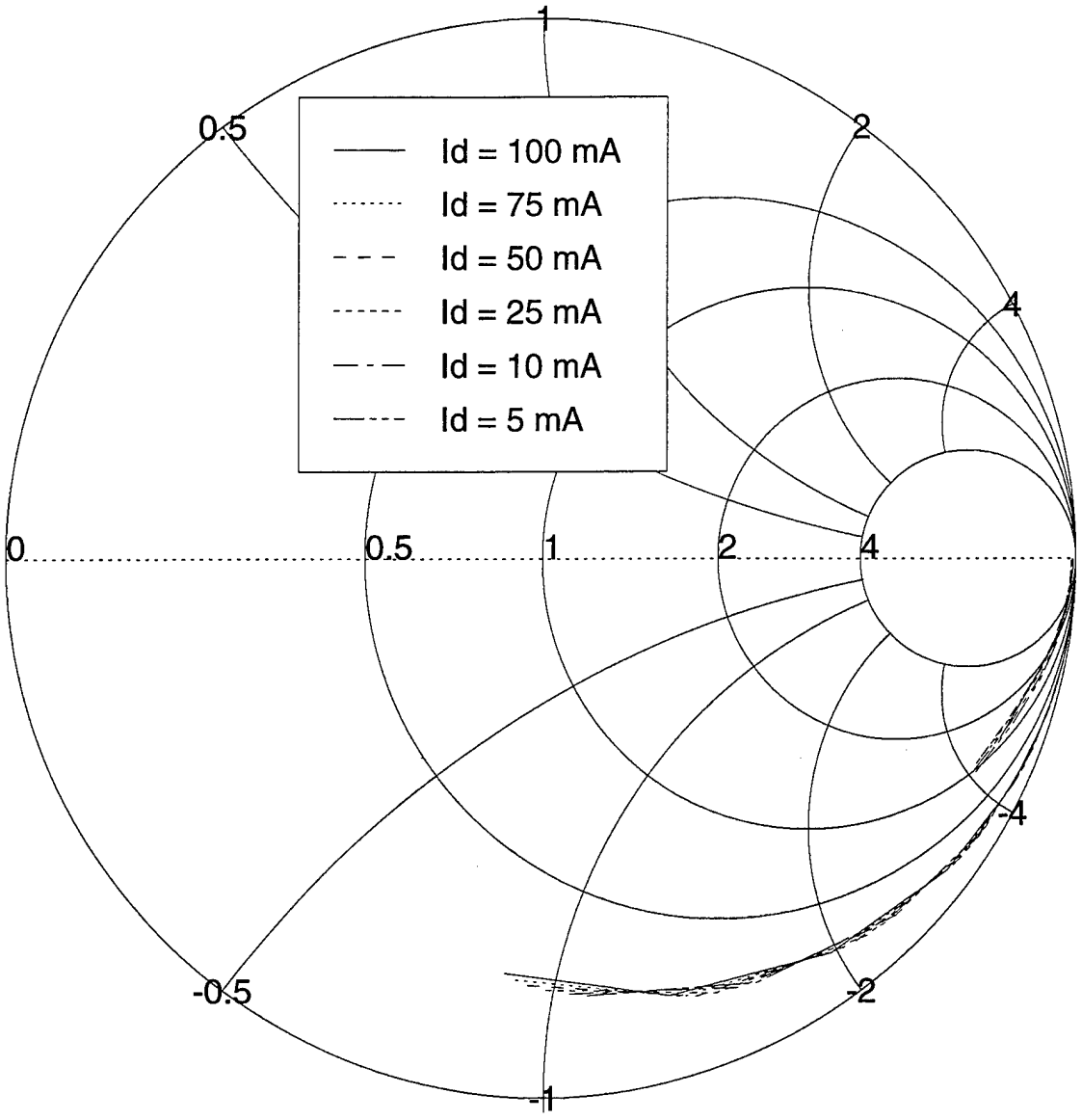

50-V RF SOI LDMOSFET (Matched)
Id-Vds curves (300K)
Vgs = 6 V
Vgs = 5 V
Vgs = 4 V
Vgs = 3 V
Vgs = 2 V
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
DRAIN CURRENT (A)
0
2
4
6
8
10
12
14
16
DRAIN VOLTAGE (V)


50-V RF SOI LDMOSFET (Matched)
Id-Vds curves (350K)
Vgs = 6 V
Vgs = 5 V
Vgs = 4 V
Vgs = 3 V
Vgs = 2 V
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
DRAIN CURRENT (A)
0
2
4
6
8
10
12
14
16
DRAIN VOLTAGE (V)


50-V RF SOI LDMOSFET (Matched)
Id-Vds curves (400K)
Vgs = 6 V
Vgs = 5 V
Vgs = 4 V
Vgs = 3 V
Vgs = 2 V
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
DRAIN CURRENT (A)
0
2
4
6
8
10
12
14
16
DRAIN VOLTAGE (V)

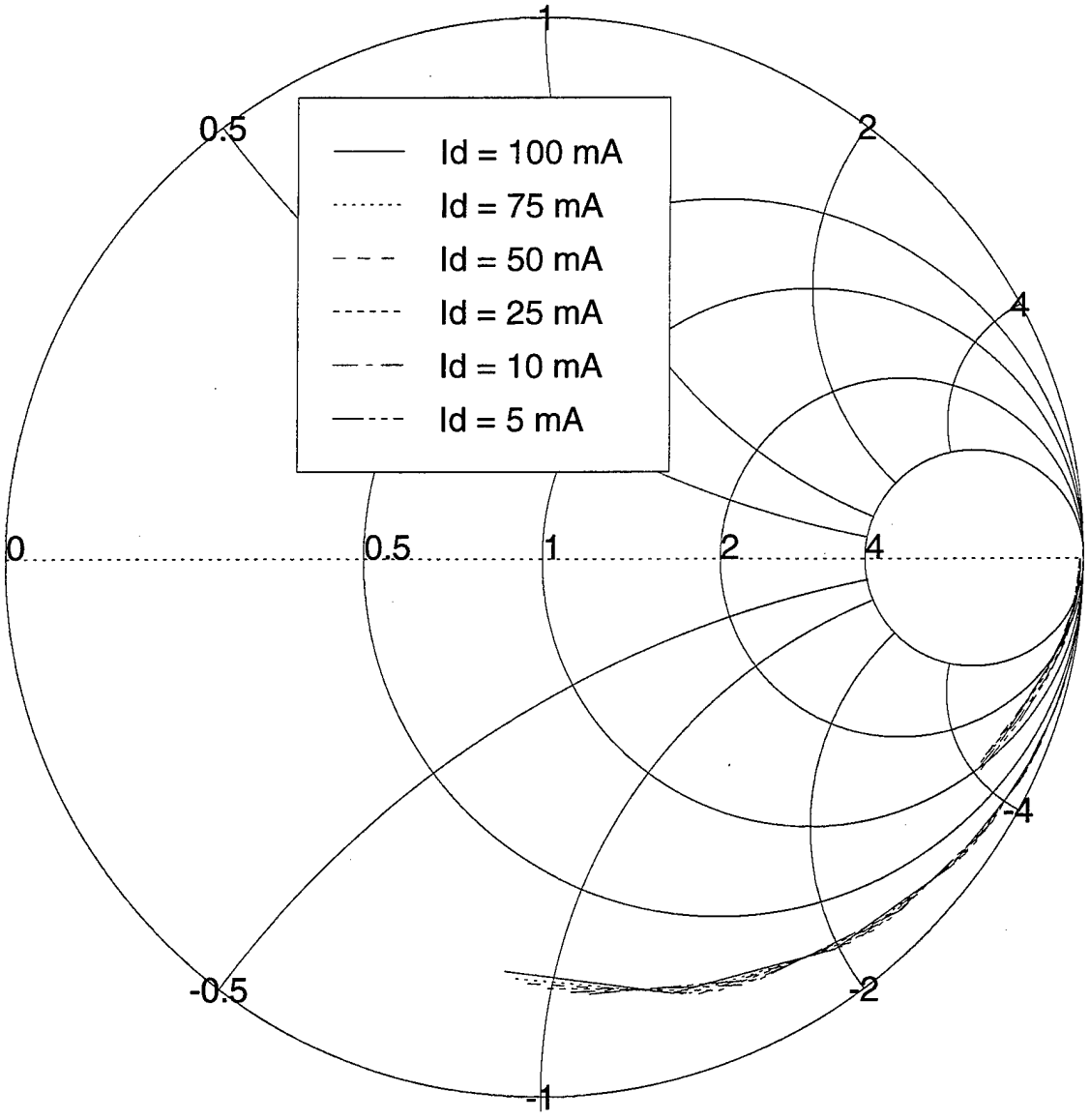
50-V RF SOI LDMOSFET (Matched)

S11 and S22 (280K)



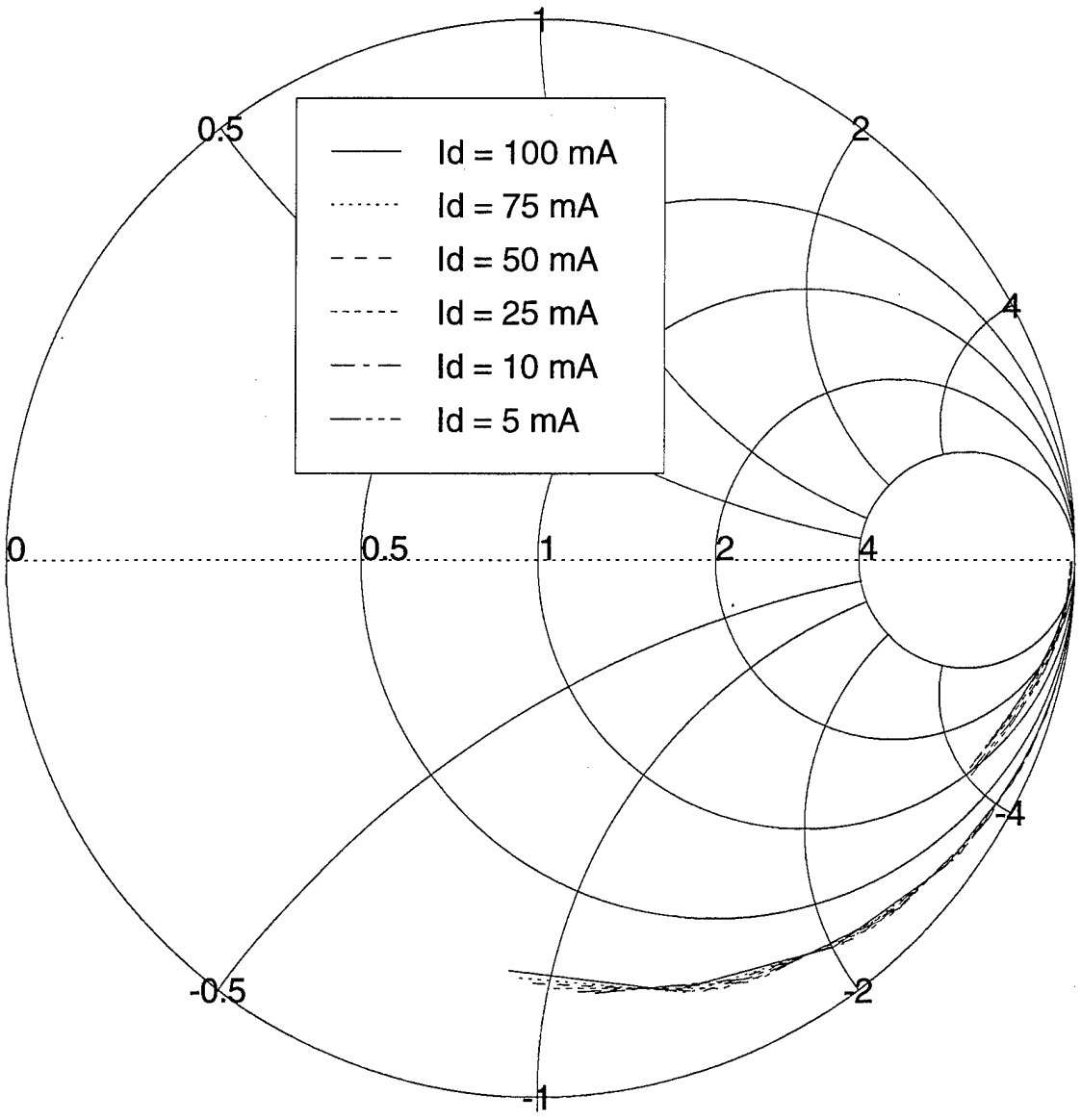
50-V RF SOI LDMOSFET (Matched)

S11 and S22 (300K)



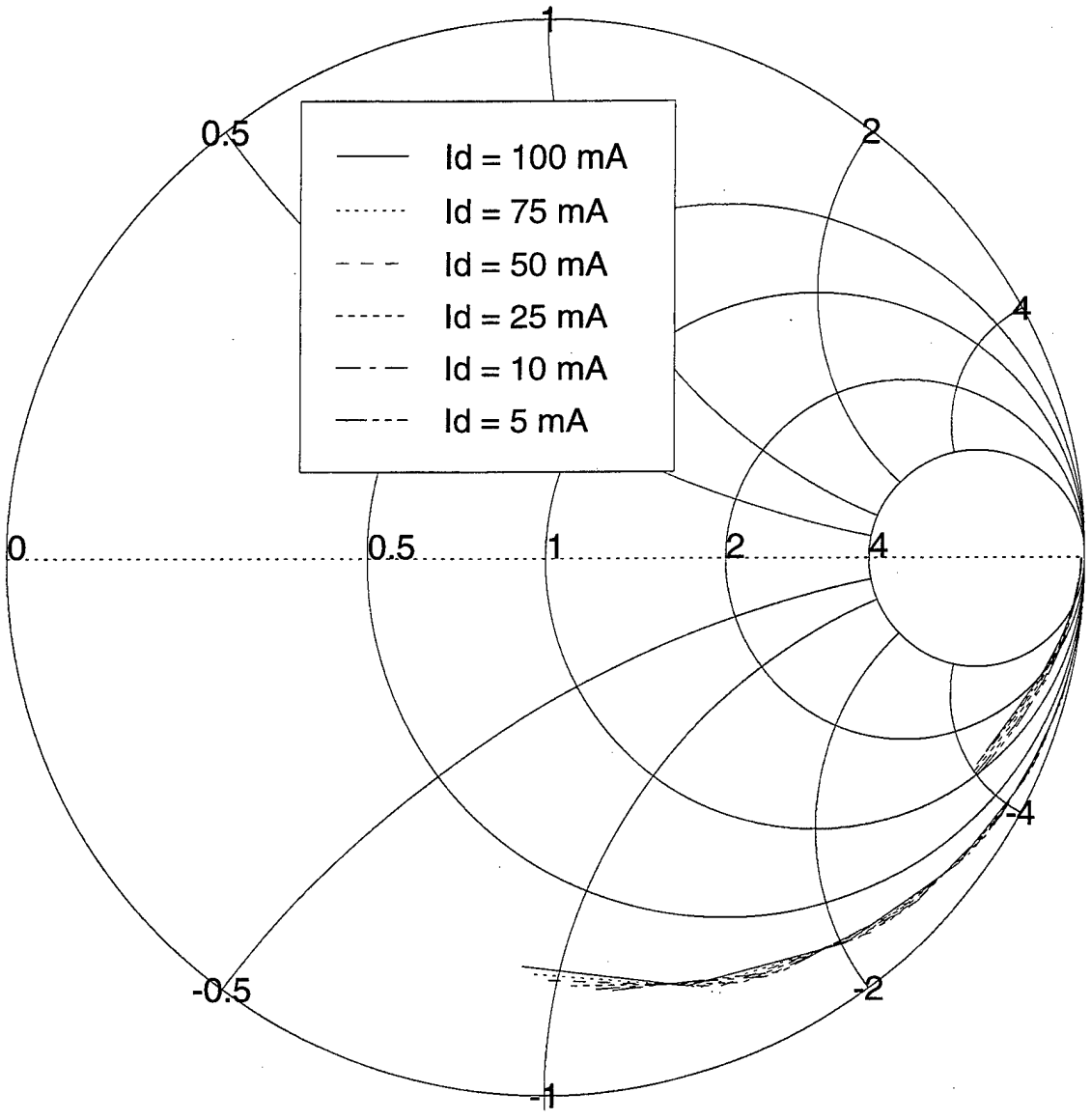
50-V RF SOI LDMOSFET (Matched)

S11 and S22 (350K)



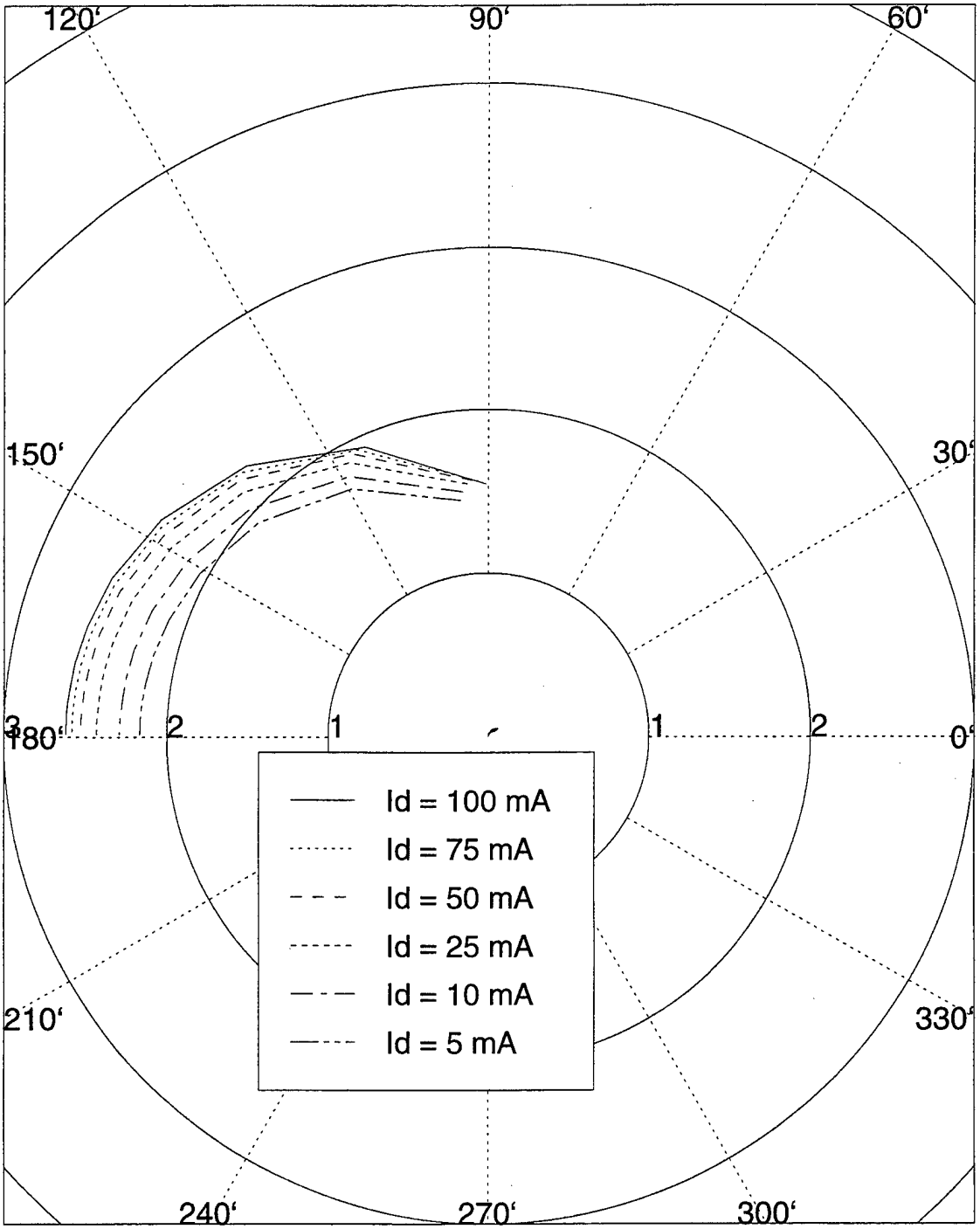
50-V RF SOI LDMOSFET (Matched)

S11 and S22 (400K)



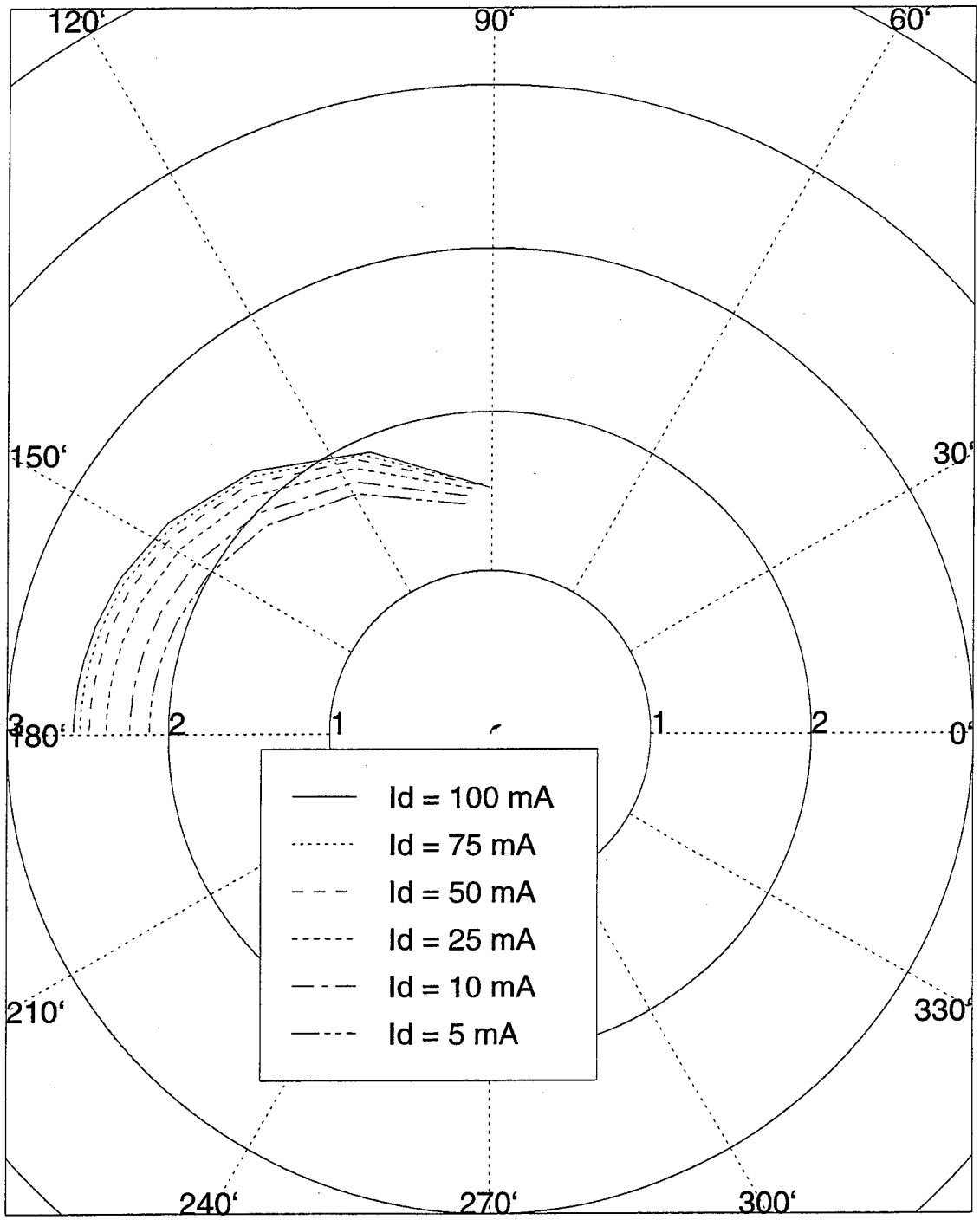
50-V RF SOI LDMOSFET (Matched)

S12 and S21 (280K)



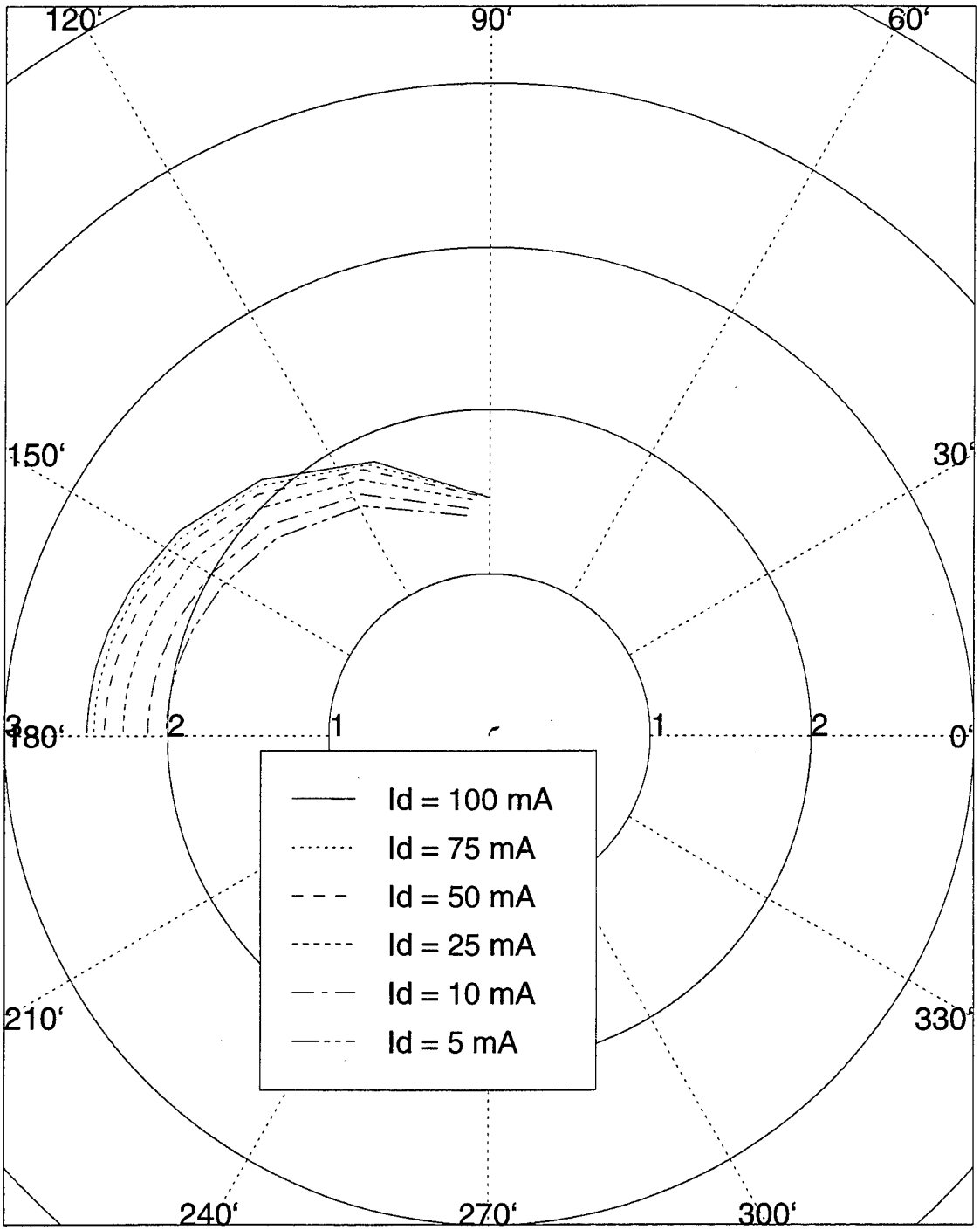
50-V RF SOI LDMOSFET (Matched)

S12 and S21 (300K)



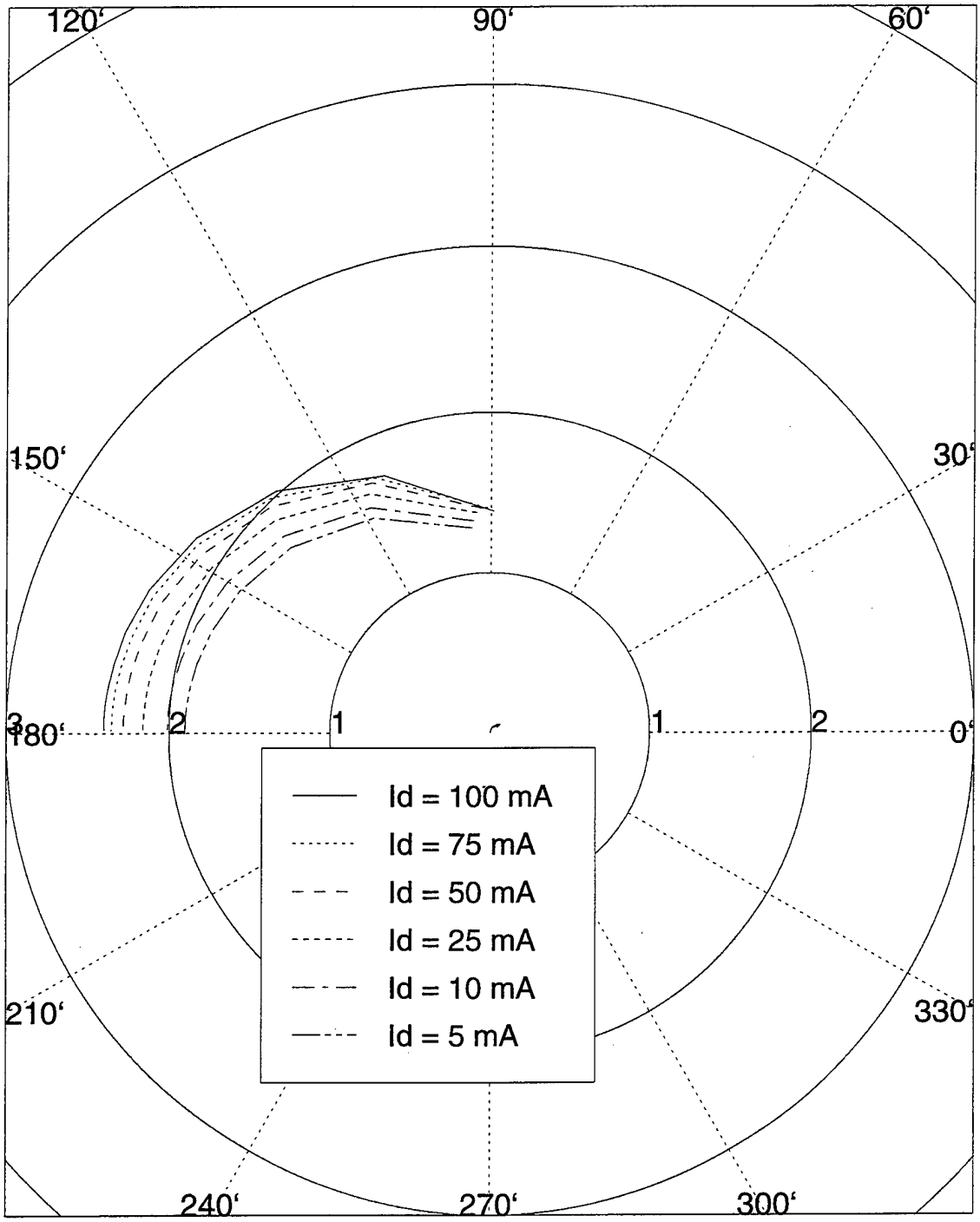
50-V RF SOI LDMOSFET (Matched)

S12 and S21 (350K)



50-V RF SOI LDMOSFET (Matched)

S12 and S21 (400K)

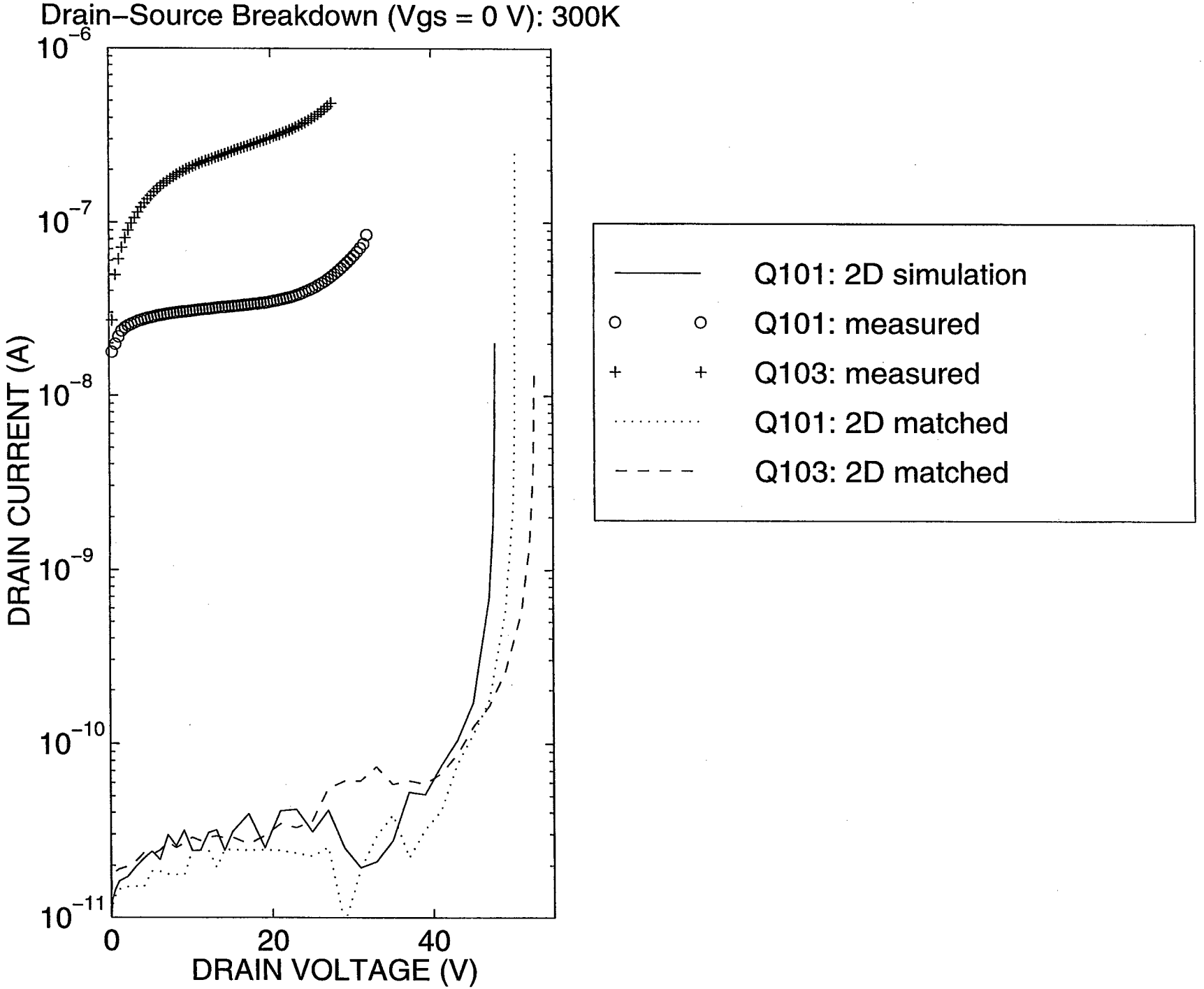


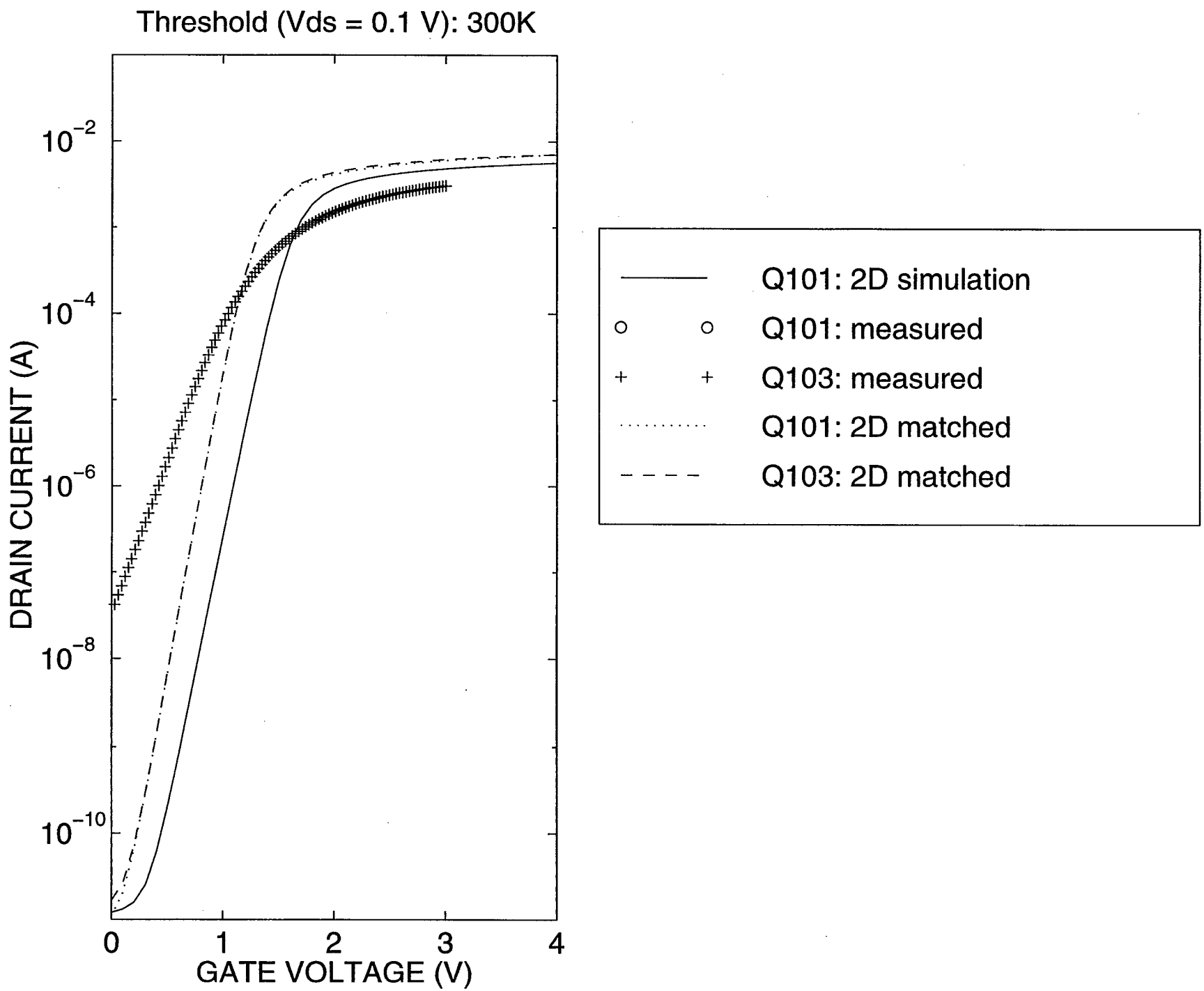
APPENDIX D

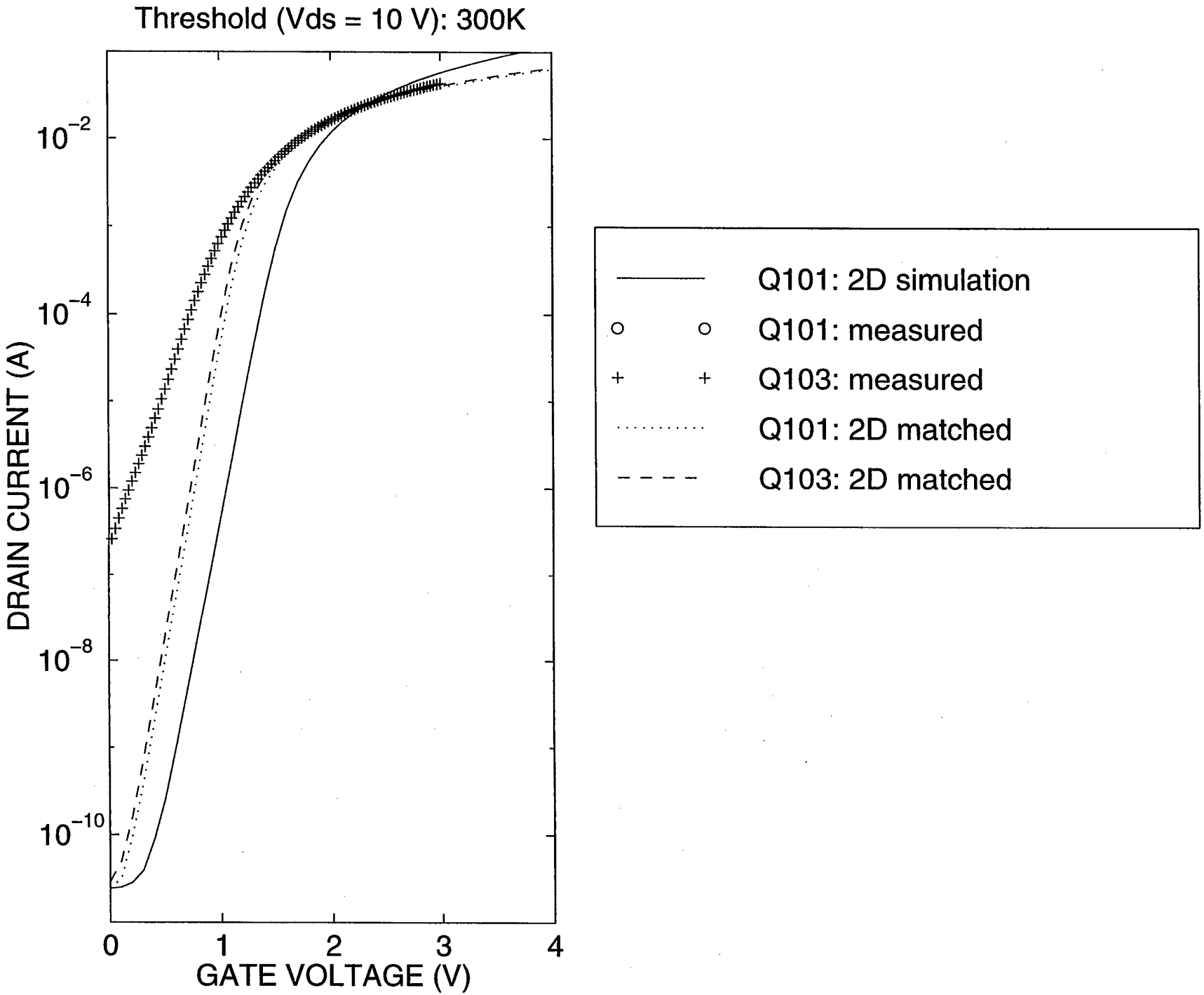
Comparison Data: Overlays of Measured, Simulated, and Modeled Results

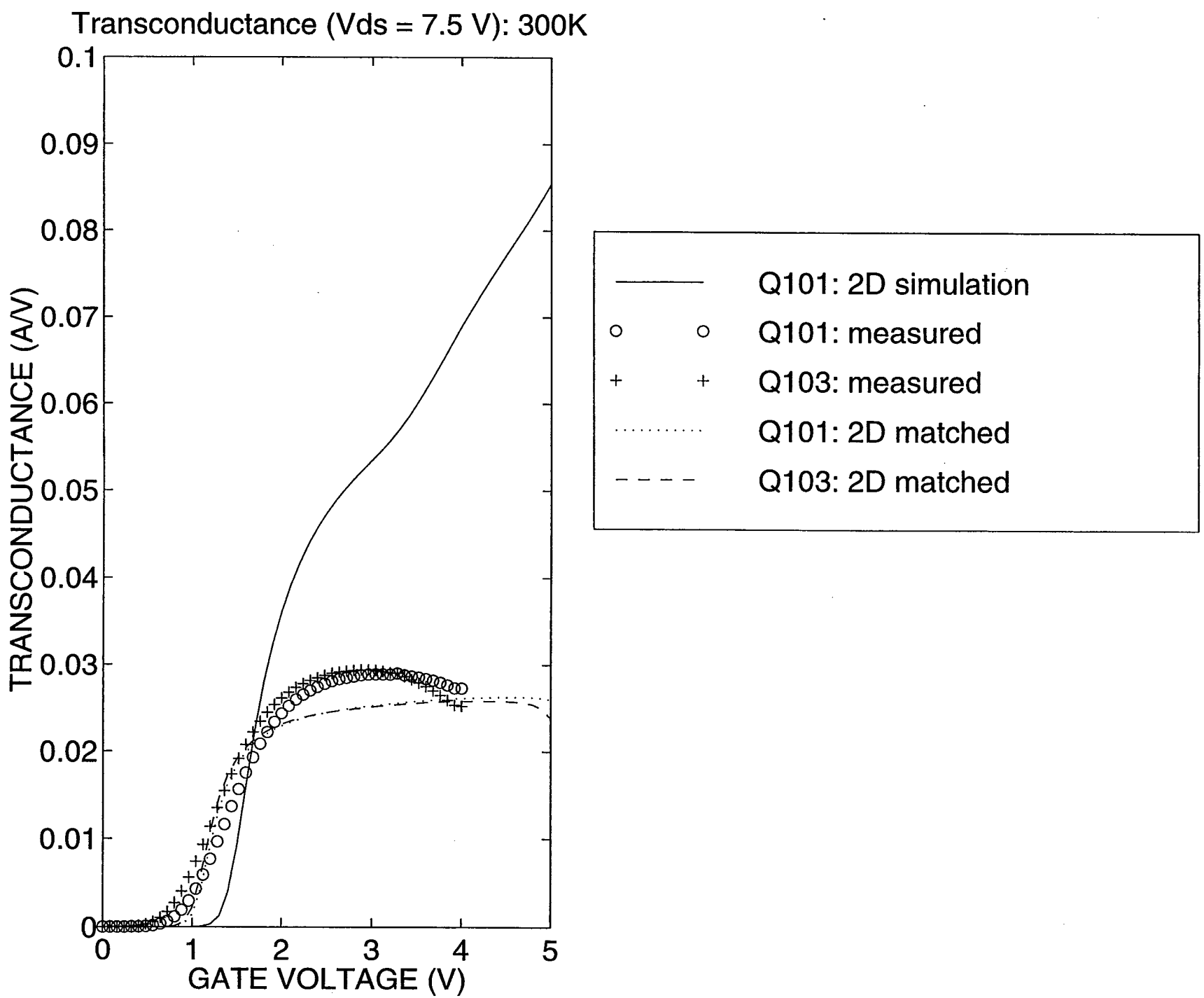
The contents of this section consist of the following waveforms. Bias conditions are noted as appropriate. Data, as noted, were obtained at 300K, 350K, and 400K.

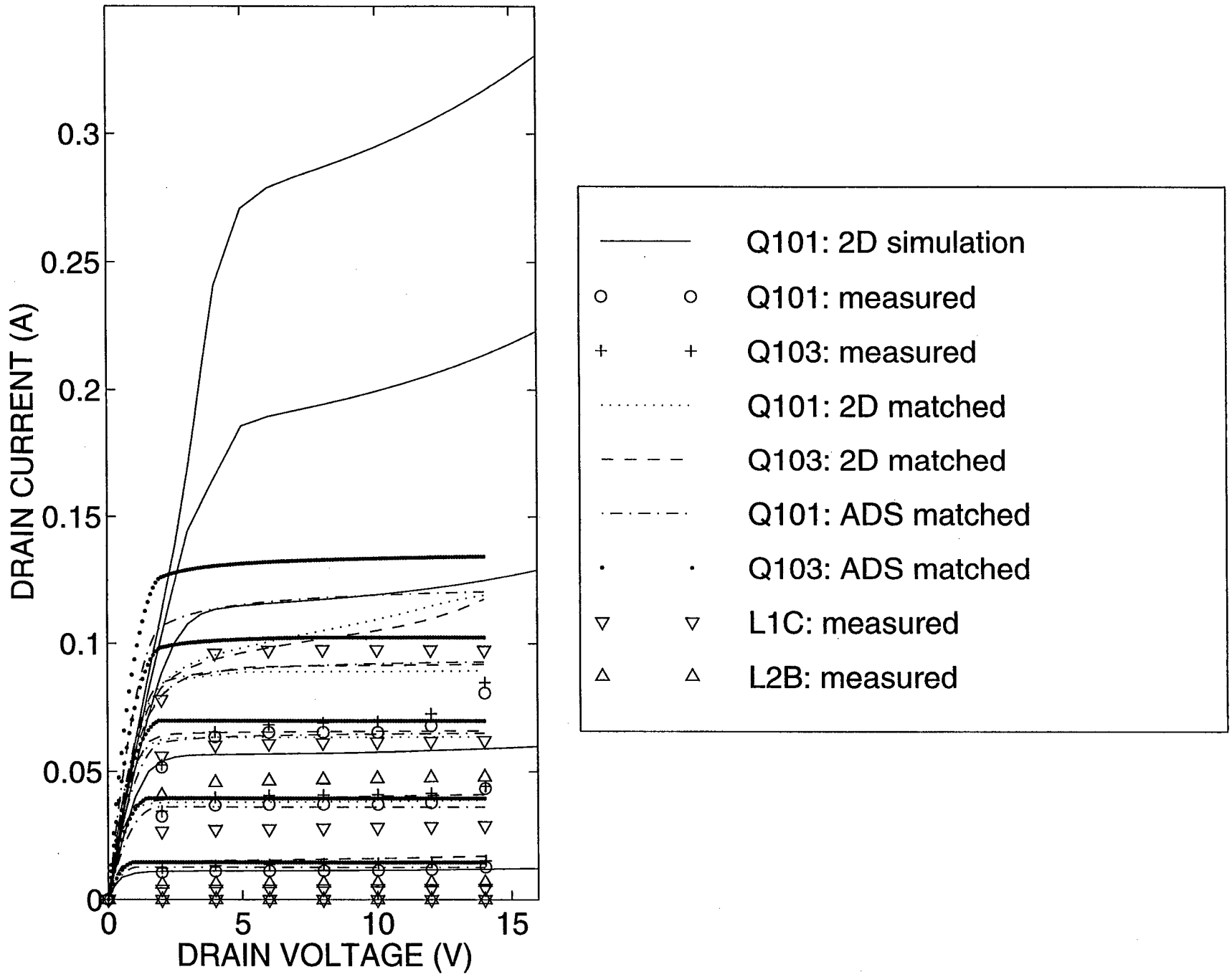
Name	**Conditions**
Drain-source static breakdown (BV_{ds})	V_{gs} = 0 V; V_{ds} = swept
Threshold voltage (V_T)	V_{ds} = 0.1,10 V; V_{gs} = 0–6 V
Transconductance versus gate bias (g_m-V_{gs})	V_{ds} = 7.5 V; V_{gs} = 0–6 V
Forward conduction (I_d-V_{ds})	V_{ds} = 0–18 V; V_{gs} = 2,3,4,5,6 V
Scattering parameters (S_{11} and S_{22})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 100 MHz – 2.1 GHz
Scattering parameters (S_{12} and S_{21})	V_{ds} = 7.5 V; I_d = 5,10,25,50,75,100 mA; f = 100 MHz – 2.1 GHz

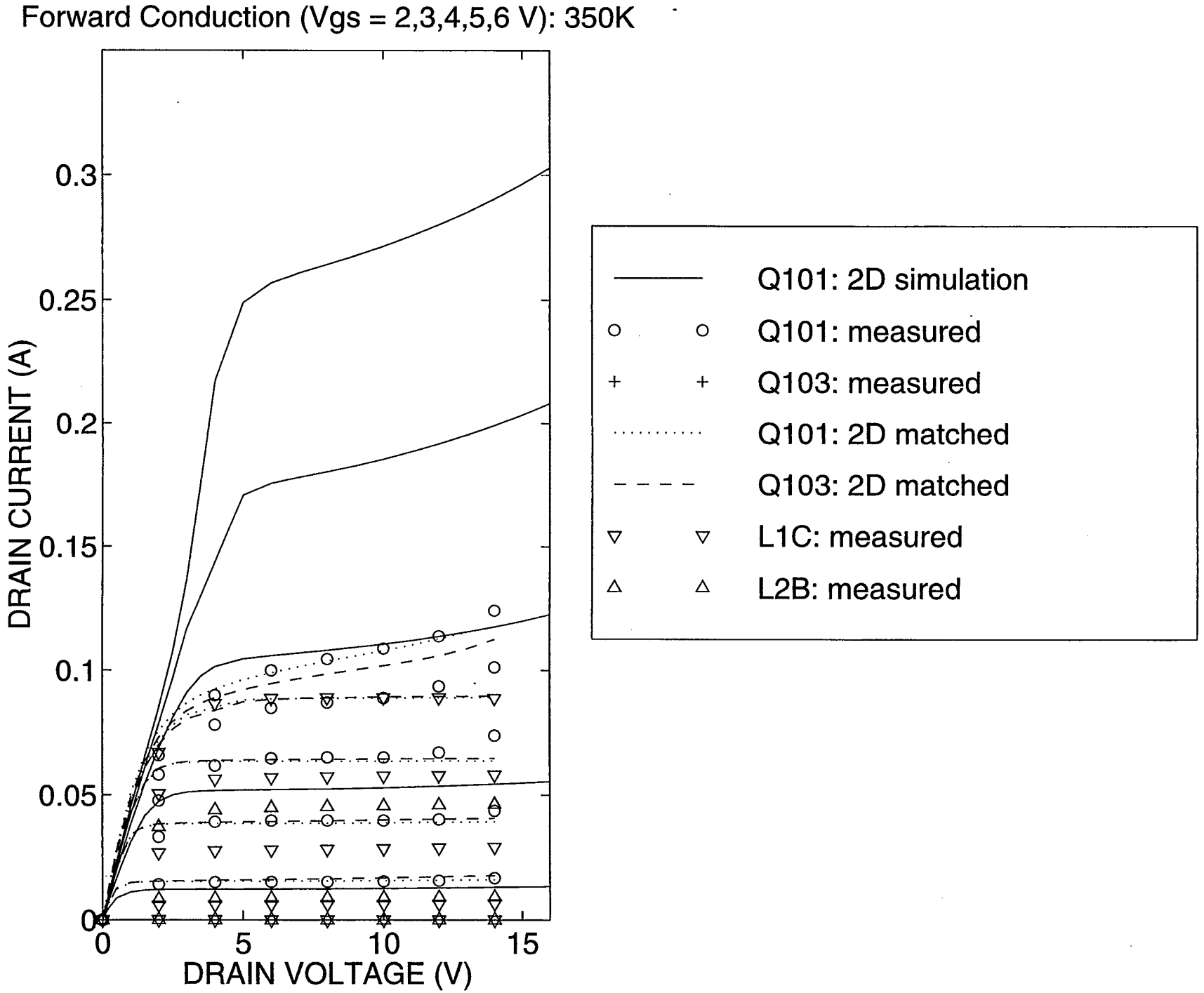

Drain–Source Breakdown (Vgs = 0 V): 300K
DRAIN CURRENT (A)
DRAIN VOLTAGE (V)
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
0
20
40
Q101: 2D simulation
Q101: measured
Q103: measured
Q101: 2D matched
Q103: 2D matched

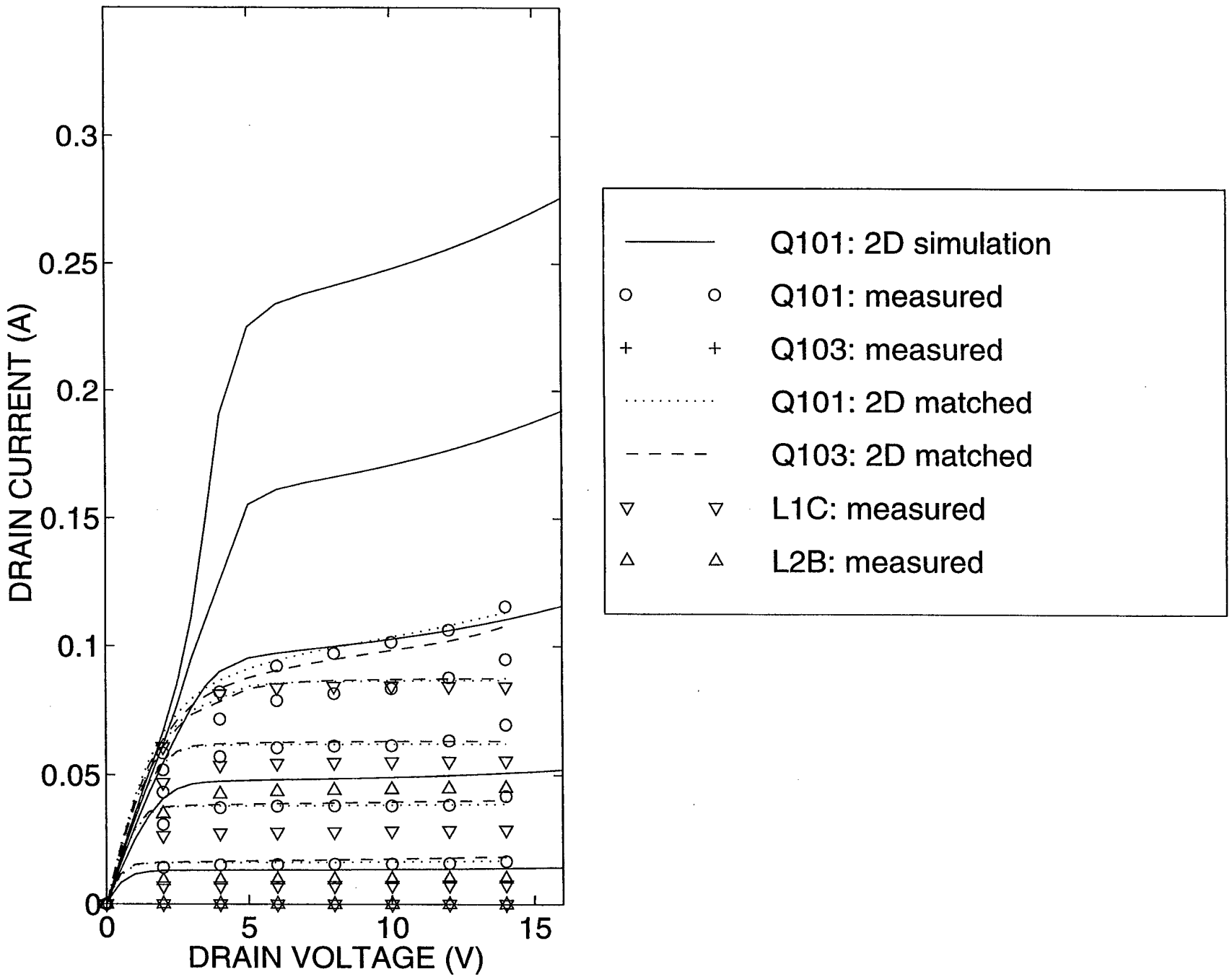

Threshold (Vds = 0.1 V): 300K
DRAIN CURRENT (A)
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
0
1
2
3
4
GATE VOLTAGE (V)
Q101: 2D simulation
Q101: measured
Q103: measured
Q101: 2D matched
Q103: 2D matched


Threshold (Vds = 10 V): 300K
DRAIN CURRENT (A)
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
0
1
2
3
4
GATE VOLTAGE (V)
Q101: 2D simulation
Q101: measured
Q103: measured
Q101: 2D matched
Q103: 2D matched

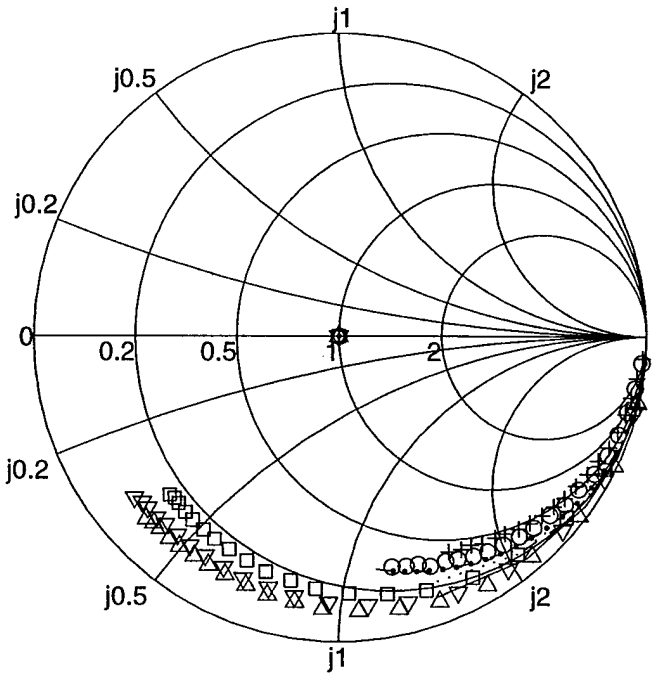

Transconductance (Vds = 7.5 V): 300K
TRANSCONDUCTANCE (A/V)
GATE VOLTAGE (V)
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
0
1
2
3
4
5
Q101: 2D simulation
Q101: measured
Q103: measured
Q101: 2D matched
Q103: 2D matched


Forward Conduction (Vgs = 2,3,4,5,6 V): 300K
DRAIN CURRENT (A)
0
0.05
0.1
0.15
0.2
0.25
0.3
0
5
10
15
DRAIN VOLTAGE (V)
Q101: 2D simulation
Q101: measured
Q103: measured
Q101: 2D matched
Q103: 2D matched
Q101: ADS matched
Q103: ADS matched
L1C: measured
L2B: measured


Forward Conduction (Vgs = 2,3,4,5,6 V): 350K
DRAIN CURRENT (A)
0
0.05
0.1
0.15
0.2
0.25
0.3
0
5
10
15
DRAIN VOLTAGE (V)
Q101: 2D simulation
Q101: measured
Q103: measured
Q101: 2D matched
Q103: 2D matched
L1C: measured
L2B: measured

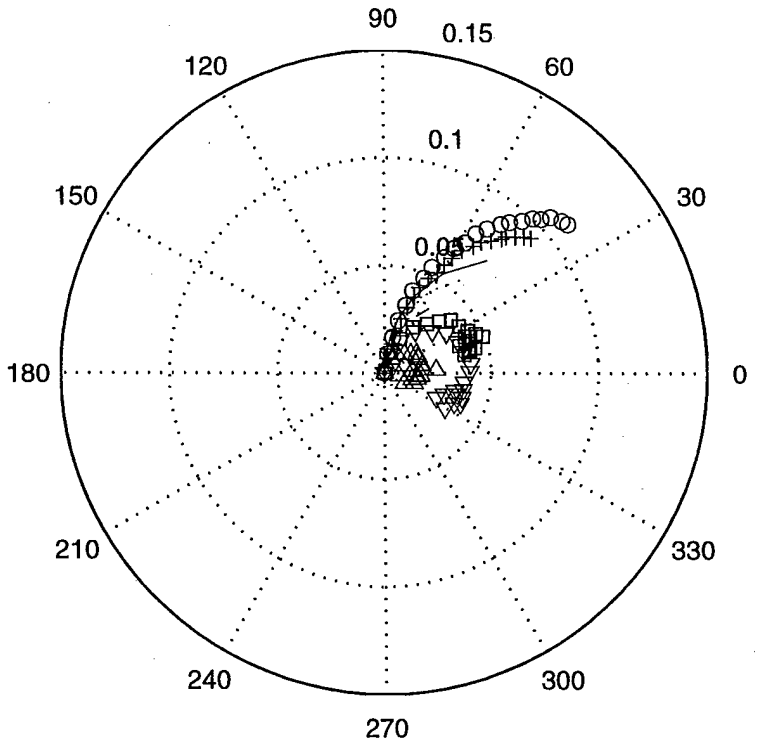

Forward Conduction (Vgs = 2,3,4,5,6 V): 400K
DRAIN CURRENT (A)
0
0.05
0.1
0.15
0.2
0.25
0.3
0
5
10
15
DRAIN VOLTAGE (V)
Q101: 2D simulation
Q101: measured
Q103: measured
Q101: 2D matched
Q103: 2D matched
L1C: measured
L2B: measured

S11 (Vds = 7.5 V, Id ~ 50 mA): 300K



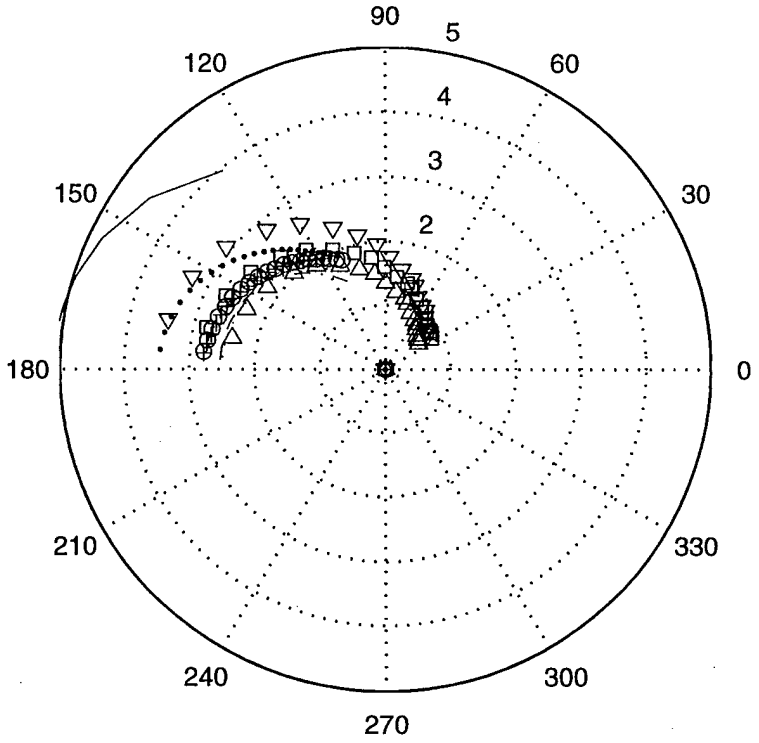
Q101: 2D simulation
Q101 (wafer): measured
Q103 (wafer): measured
Q101 (wafer): measured
Q101: 2D matched
Q103: 2D matched
Q101: ADS matched
Q103: ADS matched
L1C (packaged): measured
L2B (packaged): measured

S12 (Vds = 7.5 V, Id ~ 50 mA): 300K



Q101: 2D simulation
Q101 (wafer): measured
Q103 (wafer): measured
Q101 (wafer): measured
Q101: 2D matched
Q103: 2D matched
Q101: ADS matched
Q103: ADS matched
L1C (packaged): measured
L2B (packaged): measured

S21 (Vds = 7.5 V, Id ~ 50 mA): 300K



Q101: 2D simulation

Q101 (wafer): measured

Q103 (wafer): measured

Q101 (wafer): measured

Q101: 2D matched

Q103: 2D matched

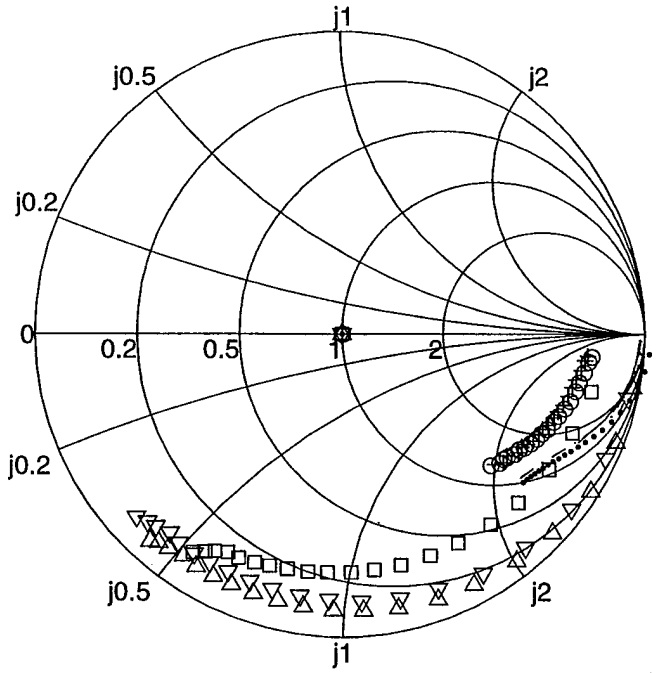
Q101: ADS matched

Q103: ADS matched

L1C (packaged): measured

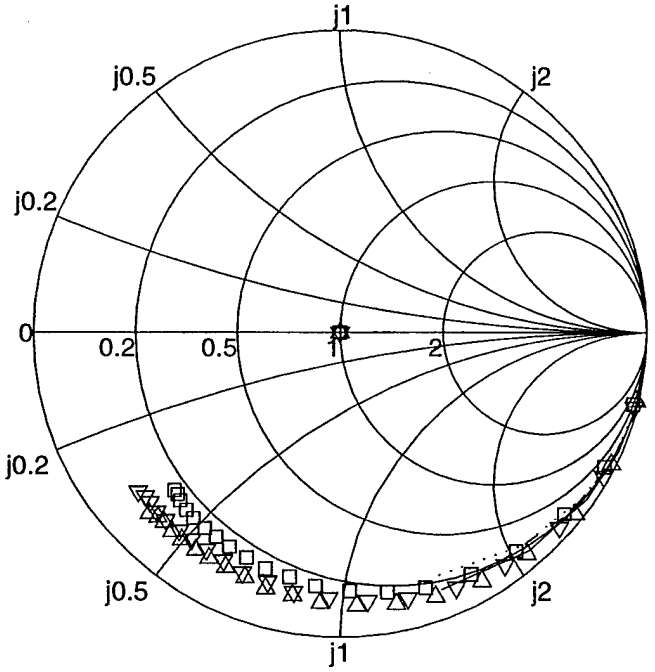
L2B (packaged): measured

S22 (Vds = 7.5 V, Id ~ 50 mA): 300K



Q101: 2D simulation
Q101 (wafer): measured
Q103 (wafer): measured
Q101 (wafer): measured
Q101: 2D matched
Q103: 2D matched
Q101: ADS matched
Q103: ADS matched
L1C (packaged): measured
L2B (packaged): measured

S11 (Vds = 7.5 V, Id ~ 50 mA): 350K



Q101: 2D simulation

Q101 (wafer): measured

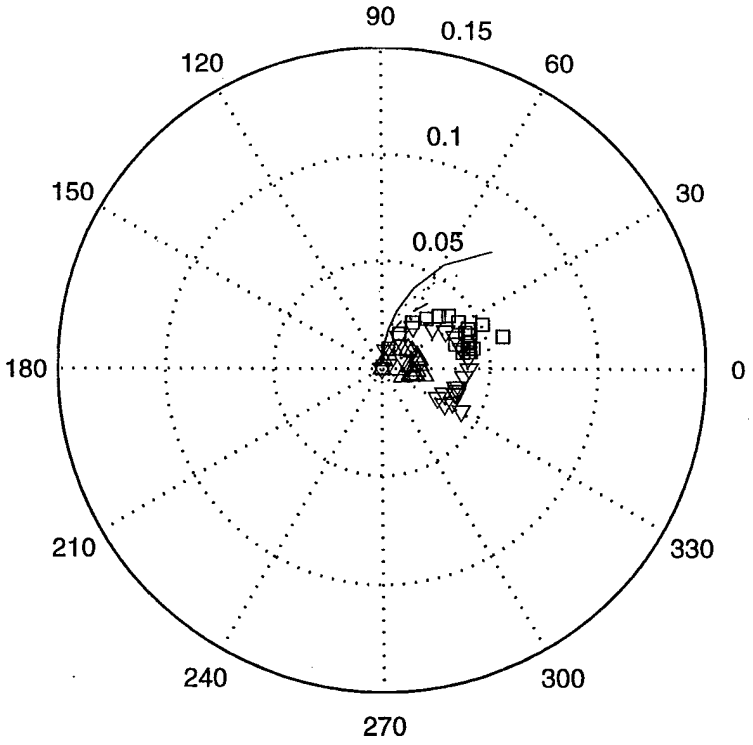
Q101: 2D matched

Q103: 2D matched

L1C (packaged): measured

L2B (packaged): measured

S12 (Vds = 7.5 V, Id ~ 50 mA): 350K



Q101: 2D simulation

Q101 (wafer): measured

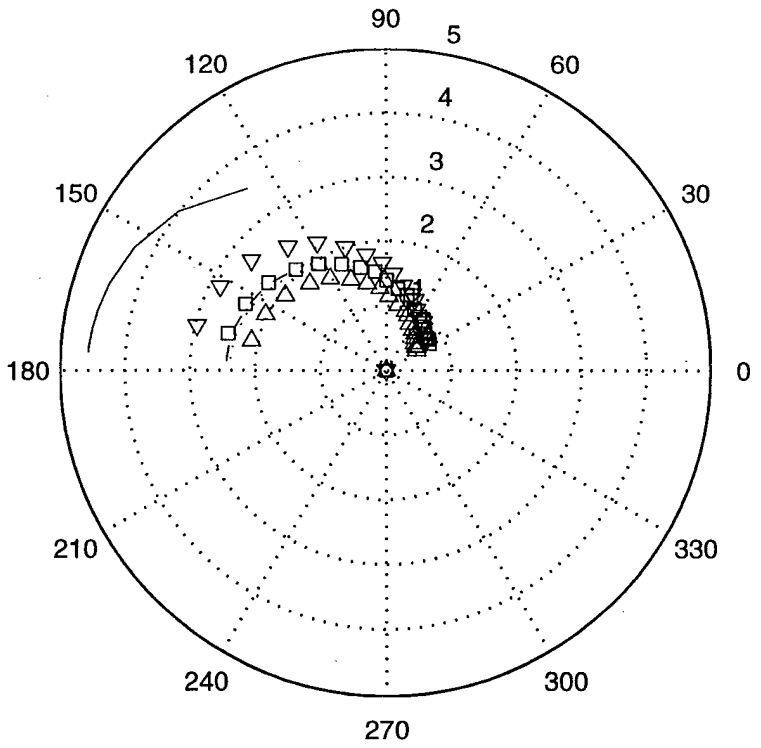
Q101: 2D matched

Q103: 2D matched

L1C (packaged): measured

L2B (packaged): measured

S21 (Vds = 7.5 V, Id ~ 50 mA): 350K



Q101: 2D simulation

Q101 (wafer): measured

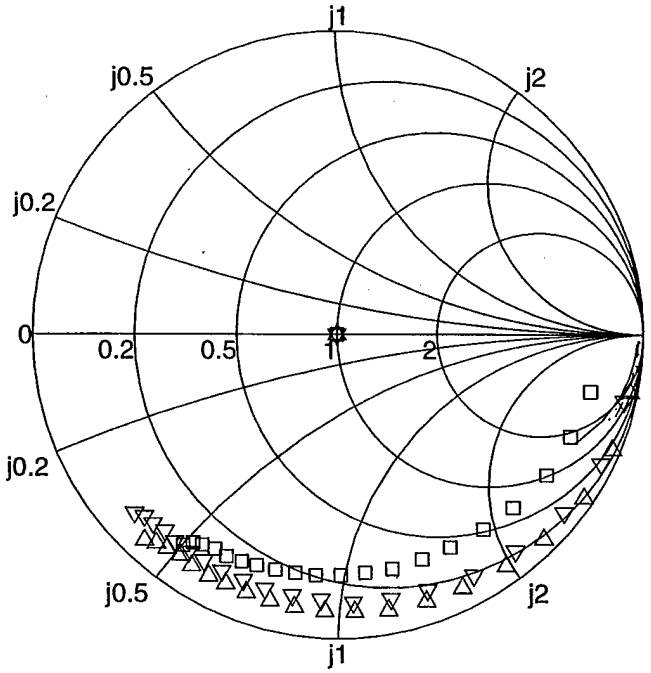
Q101: 2D matched

Q103: 2D matched

L1C (packaged): measured

L2B (packaged): measured

S22 (Vds = 7.5 V, Id ~ 50 mA): 350K



Q101: 2D simulation

Q101 (wafer): measured

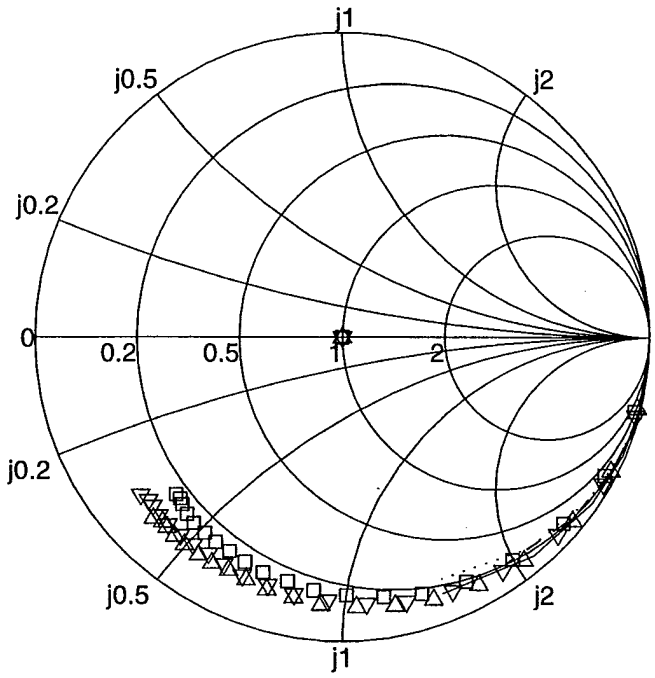
Q101: 2D matched

Q103: 2D matched

L1C (packaged): measured

L2B (packaged): measured

S11 (Vds = 7.5 V, Id ~ 50 mA): 400K



Q101: 2D simulation

Q101 (wafer): measured

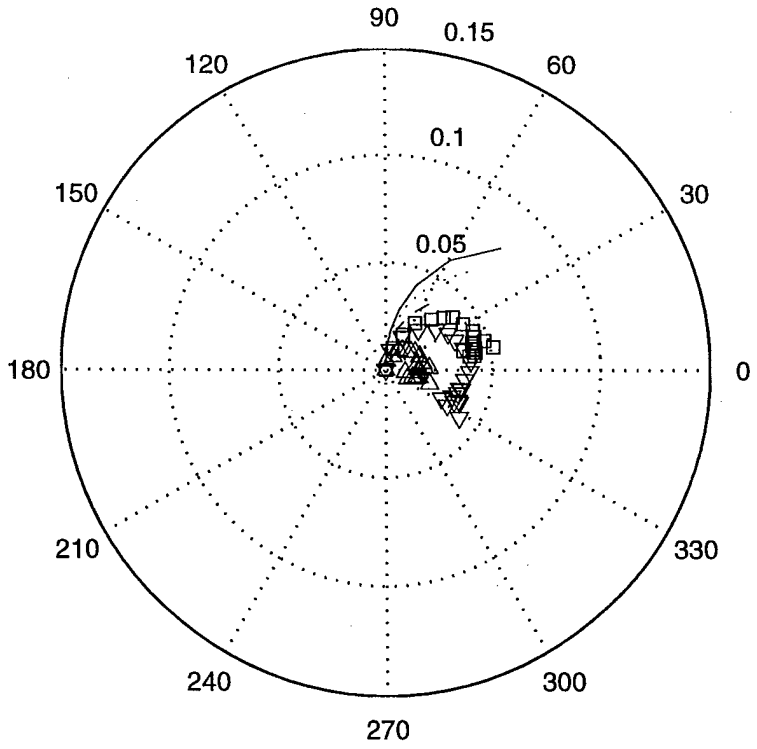
Q101: 2D matched

Q103: 2D matched

L1C (packaged): measured

L2B (packaged): measured

S12 (Vds = 7.5 V, Id ~ 50 mA): 400K



Q101: 2D simulation

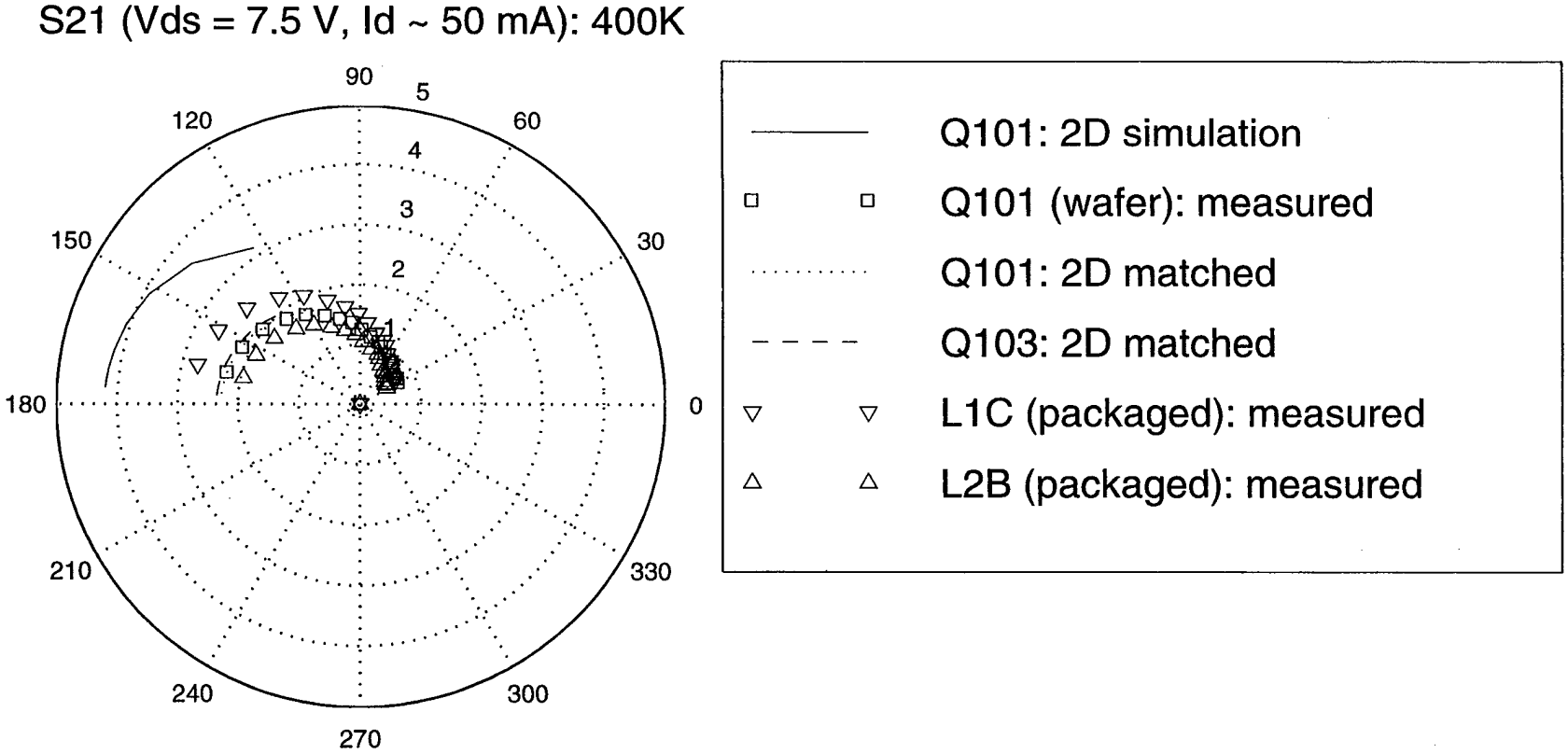
Q101 (wafer): measured

Q101: 2D matched

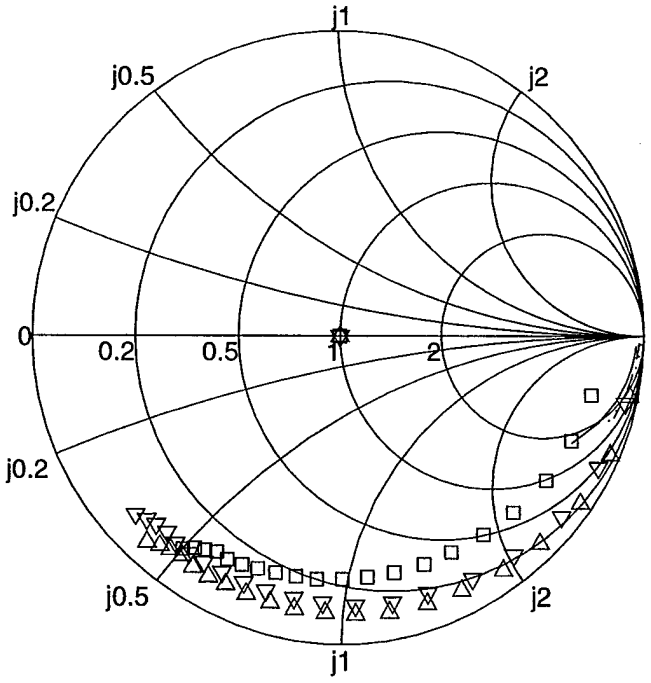
Q103: 2D matched

L1C (packaged): measured

L2B (packaged): measured


S21 (Vds = 7.5 V, Id ~ 50 mA): 400K
90
5
120
60
4
3
150
30
2
1
180
0
210
330
240
300
270
Q101: 2D simulation
Q101 (wafer): measured
Q101: 2D matched
Q103: 2D matched
L1C (packaged): measured
L2B (packaged): measured

S22 (Vds = 7.5 V, Id ~ 50 mA): 400K



Q101: 2D simulation

Q101 (wafer): measured

Q101: 2D matched

Q103: 2D matched

L1C (packaged): measured

L2B (packaged): measured